Co-Optimizing Silicon Solar Cell Processing for Efficiency and Throughput

by

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Bachelor of Engineering
Thayer School of Engineering at Dartmouth College (2011)

Submitted to the Department of Mechanical Engineering
in partial fulfillment of the requirements for the degree of

Master of Science in Mechanical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2013

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Abstract

Crystalline silicon solar cells are a proven renewable energy technology, but they have yet to reach low costs commensurate with subsidy-free, grid-scale adoption. To achieve the widespread adoption of photovoltaics, the cost per unit of electricity must be reduced by increasing solar cell efficiency. Parts per trillion concentrations of iron impurities in the silicon material can severely limit solar cell efficiency. Iron can be found in both precipitated and point defect form in silicon. Both forms are detrimental to final solar cell efficiency, but their negative impact can be mitigated during solar cell processing.

In a standard solar cell process, the phosphorus diffusion step is the key opportunity to redistribute iron impurities because because it is the step with the largest thermal budget. Phosphorus diffusion process optimization for solar cell material so far typically consists of one or more isothermal steps followed by a cooling step. Iron silicide precipitates can be dissolved at high temperatures, whereas at lower temperatures, interstitially dissolved iron is driven to the phosphorus-rich layer. Previous optimizations typically maximize minority carrier lifetime without constraining process time and device parameters.

This thesis explores a novel phosphorus diffusion process in which there are no isothermal steps. The goal of this work is to demonstrate simultaneous maximization of minority-carrier lifetime, while maintaining high process throughput and steady emitter sheet resistance. Predictive simulation, electrical characterization techniques, and synchrotron-based X-ray fluorescence were combined to compare this new processing approach to standard solar cell processing. This continuously ramped temperature processing may be a promising approach for maximizing solar cell performance, maintaining reasonable manufacturing rates, and achieving a target sheet resistance.

Thesis Supervisor: Tonio Buonassisi
Title: Associate Professor of Mechanical Engineering

Acknowledgements

A number of people have supported me personally and professionally during the past two years. I want to thank my advisor, Professor Tonio Buonassisi, for the opportunity to do research in such an exciting and relevant field and for his enthusiasm and guidance along the way.

Thanks especially to Jasmin Hofstetter and David Fenning for introducing me the numerous experimental techniques, simulations, and calculations that enable our research. David Berney Needleman and Mariela Castillo have provided critical support as lab research scientists. Thank you to Barry Lai for his expertise and assistance during synchrotron runs.

Thank you to the enthusiastic, knowledgable, and friendly postdocs and graduate students in the PVLab, especially Austin Akey, Rafael Jaramillo, Christie Simmons, Joe Sullivan, Doug Powell, Sergio Castellanos, David Berney Needleman, Rupak Chakraborty, and Riley Brandt for their encouragement, assistance, and fruitful conversations.

This research was made possible by funding from the U.S. Department of Defense's National Defense Science and Engineering Graduate Fellowship, the MIT School of Engineering SMA2 Fellowship, the National Science Foundation, and the U.S. Department of Energy.

Many thanks to Kari Jo, Janie, and Thea for keeping grounded and to my friends and family for their love and support all along the journey. Finally, thank you, Kellie.

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Chapter 1

Introduction

In light of climate change and the increasing global demand for energy, there is a clear and urgent need to increase the adoption of renewable, cost-effective utility scale energy. Solar energy is clean and abundant: "The Sun provides Earth with as much energy every hour as human civilization uses every year" [1]. Additionally, photovoltaic (PV) devices that capture and convert solar energy to usable electricity are scalable from small hand-held devices to grid-level deployment.

For replacing fossil-fuel-based electricity generation, crystalline silicon PV modules, which, as of 2011, exceed 85% of the PV market [2], have the potential to play a significant role. First of all, silicon is the second most common terrestrial element after oxygen [3]. Second, crystalline silicon absorbs efficiently because its 1.1 eV energy band gap is well matched to the peak of the solar spectrum [4]. Finally, crystalline silicon solar cell research and manufacturing builds on over sixty years of scientific, processing, equipment, and device knowledge and investment from the integrated circuit industry.

Crystalline silicon PV is a proven technology with a record efficiency research laboratory single crystal non-concentrating silicon solar cell fabricated by the University of New South Wales (UNSW) achieving over 25% efficiency [5] and Sunpower commercially available modules for residential applications exceeding 21.5% [6]. However, PV has much room to grow. In 2012 in the United States, just 1% of electricity was generated from solar energy, and between 2000 and 2011, the amount of electricity

generated from solar energy in the United States more than doubled [7, 8]. The U.S. Department of Energy's SunShot Initiative was launched in 2011 to accelerate the adoption of solar energy in the U.S with the goal of 14% of electricity from solar by 2030. Its SunShot Vision Study projects that solar energy will reach grid parity "when the price of solar electricity reaches about $0.06 per kilowatt-hour over its lifetime" [9].

The module cost is sensitive to solar cell efficiency and the cost of silicon feedstock, labor, and depreciation as shown in Fig. 1-1. The key to driving down the cost, and subsequently the price, of crystalline silicon PV is maximizing the efficiency of photovoltaic modules due to the area-dependence of the cost of solar module materials and installation [10]. Given this cost structure, this research aims to maximize crystalline silicon solar cell efficiency through process innovation while maintaining a high rate of manufacturing throughput.

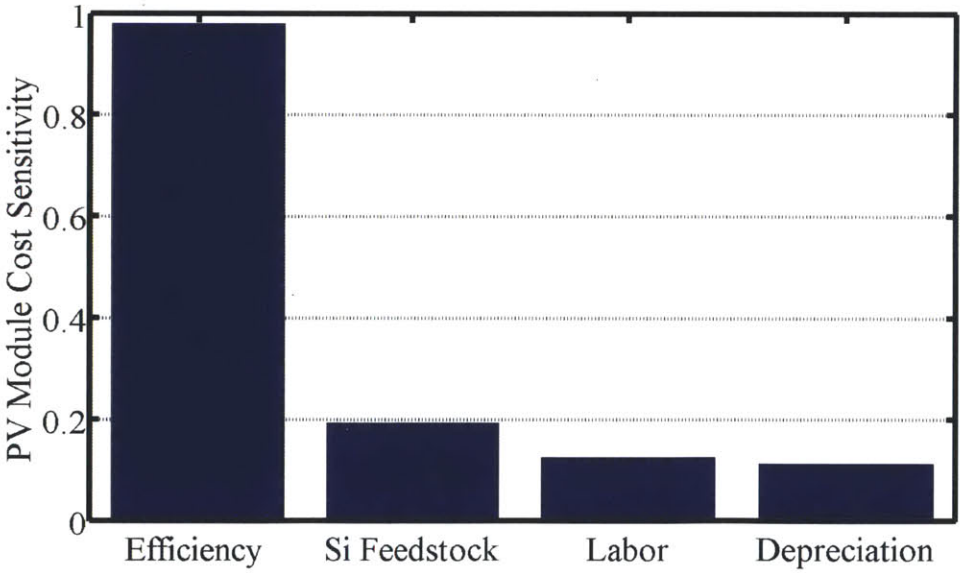

Figure 1-1: The cost of a PV module is most sensitive to solar cell efficiency followed by the costs of silicon feedstock, labor, and depreciation.

Minute concentrations of iron impurities, found in precipitated and point defect form in silicon, can severely limit solar cell efficiency, but iron's negative impact can

be mitigated during solar cell processing.

In a typical silicon solar cell process, the phosphorus diffusion step is the key opportunity to redistribute iron impurities because it is the longest high temperature step. Phosphorus diffusion process optimization for solar cell material typically consists of one or more isothermal steps followed by a cooling profile. Previous optimizations typically maximize minority carrier lifetime without constraining process time and device parameters.

This thesis explores a novel phosphorus diffusion processing profile shape in which there are no isothermal steps. Predictive simulation, electrical characterization techniques, and synchrotron-based X-ray fluorescence spectroscopy were combined to compare this new processing approach to standard solar cell processing. This continuously ramped temperature processing may be a promising approach for increasing solar cell efficiency while maintaining reasonable manufacturing rates and achieving a target sheet resistance, an important solar cell device parameter.

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Chapter 2

Crystalline Silicon Photovoltaics Theory and Background

Crystalline silicon solar cell efficiency is governed by the minority carrier lifetime, an important electronic parameter of a silicon wafer. Impurities and structural defects in silicon material can decrease the minority carrier lifetime. A particularly lifetime-limiting impurity, iron is abundant in semiconductor manufacturing environments [11]. It can diffuse rapidly into silicon wafers and limit the lifetime of wafers and final solar cell efficiency. This research focuses on mitigating the negative impact of iron on solar cell efficiency through optimized solar cell processing.

2.1 Effect of Iron Impurities on Crystalline Silicon Solar Cell Efficiency

The efficiency of a solar cell is the ratio of the output power to the input power from the sun. For standard crystalline silicon solar cells, both the voltage and the current output of the solar cell depend on the diffusion length of charge carriers. The diffusion length is the average distance that a charge carrier travels before recombining, and it increases with diffusivity and carrier lifetime. The effective minority carrier lifetime is the harmonic sum of the carrier lifetimes determined by each type of recombination

present in the material as shown in Eq. 2.1 . Most commonly, charge carriers can recombine at impurities due to Shockley-Read-Hall recombination, at wafer surfaces, and in heavily-doped material due to Auger recombination [12].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surf}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{other}} \tag{2.1}$$

Thus, all else held equal, for multicrystalline silicon solar cells with a standard architecture that is lifetime limited, increasing the lifetime of charge carriers in silicon wafers through optimized solar cell processing increases final solar cell efficiency [12]. Assuming a typical solar cell device architecture and material parameters, the relationship between solar cell efficiency and minority carrier lifetime was simulated using the open-source software *PC1D* and is shown in Fig. 2-1 [13]. In this case, varying the bulk minority carrier lifetime from 5 to 100 μs resulted in a range of solar cell efficiencies from 14.5 to 17.75%. Initially, efficiency rapidly increases as lifetime increases, but at higher lifetimes, the efficiency saturates as other solar cell device parameters limit the efficiency.

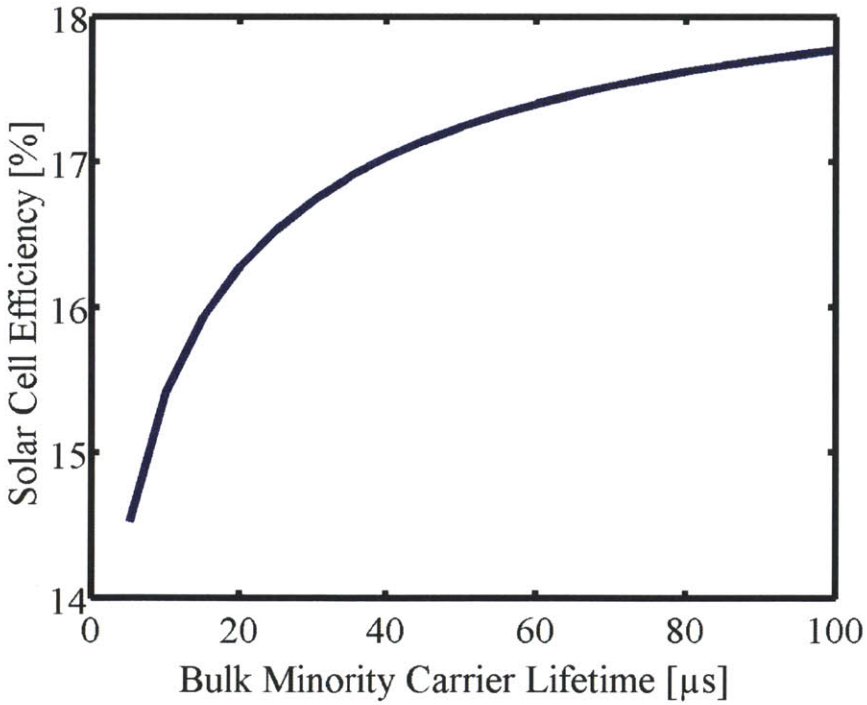


Figure 2-1: Standard silicon solar cell efficiency increases with minority carrier lifetime

In silicon, iron exists as point defects or in metallic precipitates. Iron in both of these chemical states reduces minority carrier lifetime, but point defects are especially detrimental because they are almost always found in higher concentrations than precipitated defects [14]. Precipitates are recombination active, and they also are sources and sinks for interstitial iron. Thus, it is essential to manage both iron point defects and precipitates during solar cell processing.

In boron-doped silicon wafers, iron point defects can be found either in positively charged interstitial form (Fe_i) or paired with boron in iron-boron pairs (Fe-B). The allowed energy levels for Fe_i and Fe-B are between the valence band and the conduction band energy levels [15]. Shockley-Read-Hall recombination due to impurities is maximum for energy levels at approximately mid-gap [16, 17]. Thus, iron and other impurities that introduce allowed energy levels near the middle of the energy band gap can be especially detrimental to charge carrier lifetime and final solar cell efficiency. The decrease in lifetime due to increasing concentrations of Fe_i and Fe-B pairs, shown in Figure 2-2, was simulated assuming Shockley-Read-Hall statistics with a boron doping concentration of 10^{16} cm^{-3} and an injection level of 10^{15} cm^{-3}. Interstitial iron at even parts per trillion (approx. 5.5×10^{10} cm^{-3}) and parts per billion (approx. 5.5×10^{13} cm^{-3}) can negatively impact solar cell performance.

Although iron point defects are usually more detrimental than iron precipitates in p-type silicon, iron precipitates are also recombination active. Gundel *et al.* found that because silicon has a strong piezoresistance, tensile stress is positively correlated with recombination activity of precipitates [18]. In another approach by del Cañizo and Luque inspired by Plekhanov and Tan, recombination at precipitates can be modeled by Eq. 2.2 where r is the precipitate radius, N is the precipitate density, τ_{ppt} is the minority carrier diffusion length in silicon, and s is the surface recombination velocity at the surface of the precipitate [19, 20].

$$\frac{1}{\tau_{ppt}} = 4\pi^2 N \frac{\frac{sD}{r}}{s + \frac{D}{r}} \tag{2.2}$$

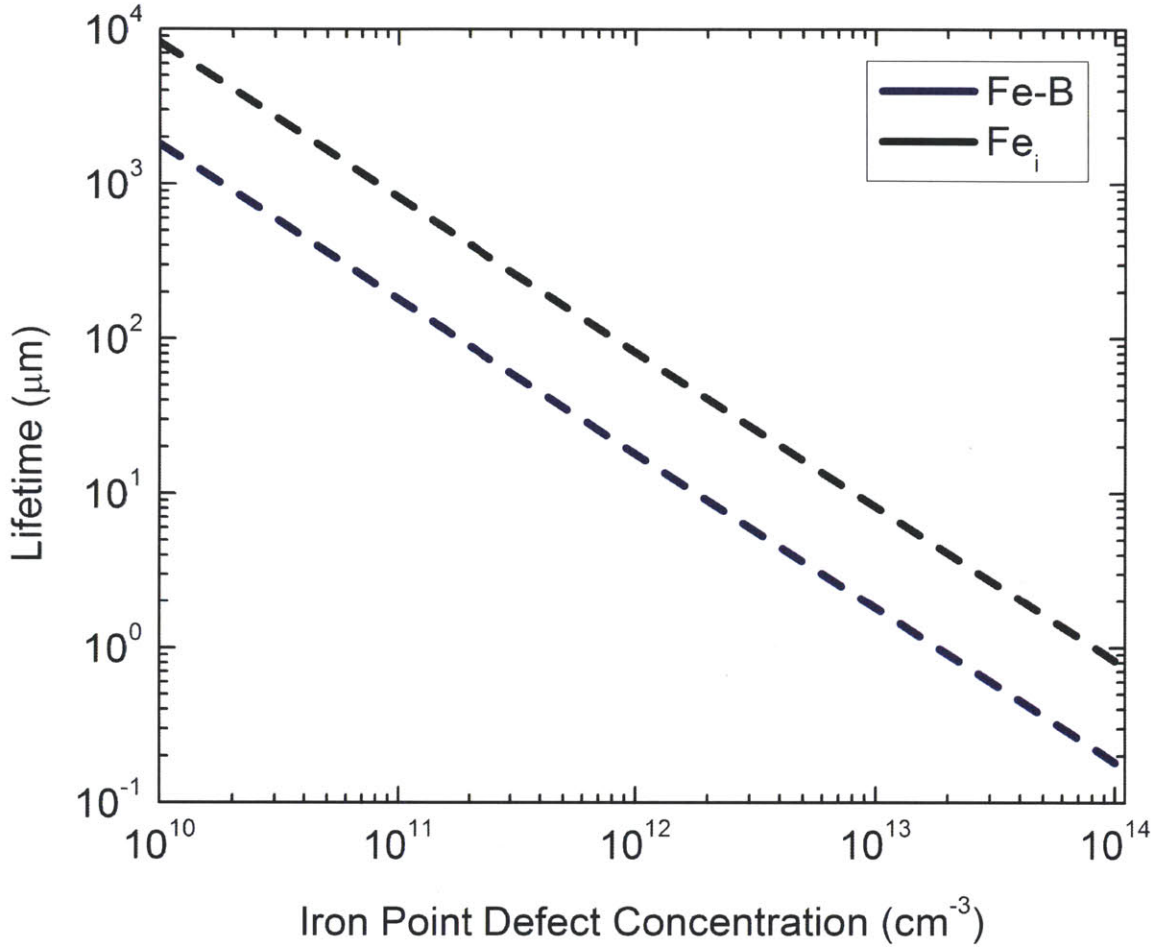


Figure 2-2: Lifetime decreases as iron point defect concentration increases. For a given concentration, Fe-B pairs are less detrimental than Fe_i. An injection level of 10^{15} $cm^{-3}$was assumed.

2.2 Mitigating the Negative Impact of Iron During the Solar Cell Fabrication Process

Because iron is almost always present in detrimental concentrations in as-grown silicon wafers for solar cells, it is important to mitigate the negative impact of iron during the solar cell processing. It is ideal to optimize a step that is already necessary for solar cell manufacturing in order to keep production rate high and cost down.

A basic silicon single-junction solar cell can be manufactured in four steps, two of which are at high temperature. A cross-section of such a solar cell is represented in Fig. 2-3(a), and the time temperature profile of the process is shown in Fig. 2-3(b).

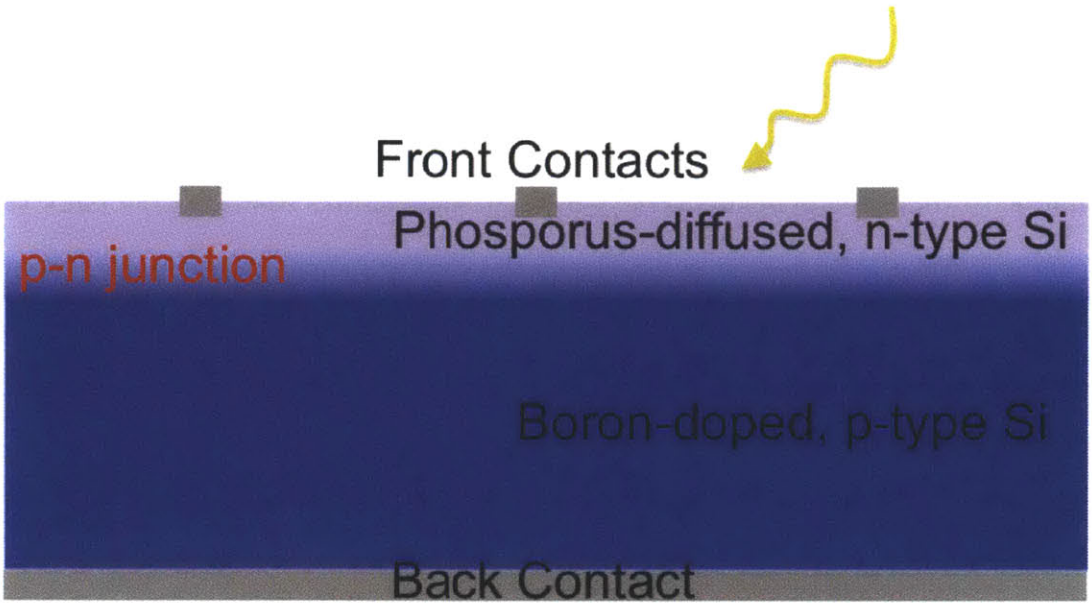
The input to the process is a boron-doped silicon wafer, represented in blue. The first step is to form a p-n junction by heating the wafer to around 840°C, in-diffusing phosphorus, represented by purple shading, into the surface of the wafer, and then cooling it to room temperature. The p-n junction separates electron-hole pairs that have been generated by photos from the sun, denoted by the yellow arrow. The second and third steps, done at room temperature, are to deposit electrical contacts, denoted by the grey rectangles, on the front and back of the solar cell in order to allow the excited charge carriers to flow to an external circuit. Finally, the solar cell is fired at approximately 800°C for a few seconds so the metal contacts make electrical contact with the silicon.

To redistribute iron, the silicon material must be at high temperatures for some extended amount of time. The diffusion length of iron during processing can be approximated as the square root of the product of the process time and the diffusivity of iron in silicon. The diffusivity of iron in silicon increases exponentially with temperature. Thus, the phosphorus diffusion step is the key opportunity during the solar cell process to redistribute iron.

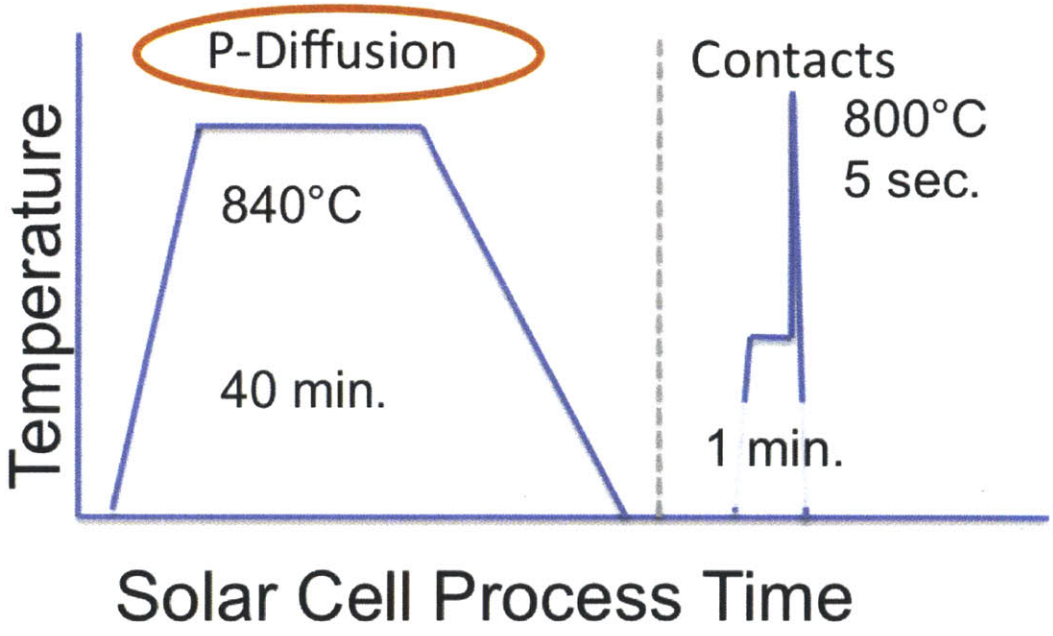
In order to maximize solar cell efficiency, iron must be removed from the bulk boron-doped silicon into the phosphorus-diffused layer. Iron is less detrimental in the phosphorus-diffused emitter because it is electrically neutral in n-type material, and it has a smaller capture cross section for holes in n-type material than in p-type material. Additionally, the lifetime in the emitter is typically limited by Auger recombination due to the high concentration of phosphorus rather than Shockley-Read-Hall recombination due to impurities [12].

2.3 Phosphorus Diffusion Gettering Mechanisms

In the context of mitigating iron in silicon for solar cells, gettering is the redistribution of iron to metallic precipitates, structural defects, and the phosphorus-rich emitter. A typical solar cell phosphorus diffusion process has three temperature steps as shown in Figure 2-4. In the first step (1), as the wafers heat up, if they are present, iron pre-



(a) Cross-section of solar cell



(b) Time-temperature profile of a basic solar cell process. The phosphorus diffusion step is the key opportunity to reduce the detrimental impact of iron impurities during processing (adapted from [21]).

Figure 2-3: Schematic of a basic solar cell and the time temperature profile of the process

cipitates dissolve because the solubility of iron in silicon increases exponentially with temperature [15]. In the middle high-temperature isothermal step (2), phosphorus

diffuses into the surface of the wafers, and precipitates, if any, continue to dissolve, increasing the concentration of iron point defects. Additionally, iron point defects are highly mobile because the diffusivity of iron increases exponentially with temperature, and they move toward the emitter because the solubility of iron in phosphorus-rich silicon is higher than that in boron-doped silicon [15, 22]. Finally, during the cooling step (3), dissolution of precipitates decreases and the segregation coefficient, the ratio of the solubility of iron in the phosphorus layer to that in the boron-doped region increases, increasing the driving force of iron point defects from the bulk to emitter [22].

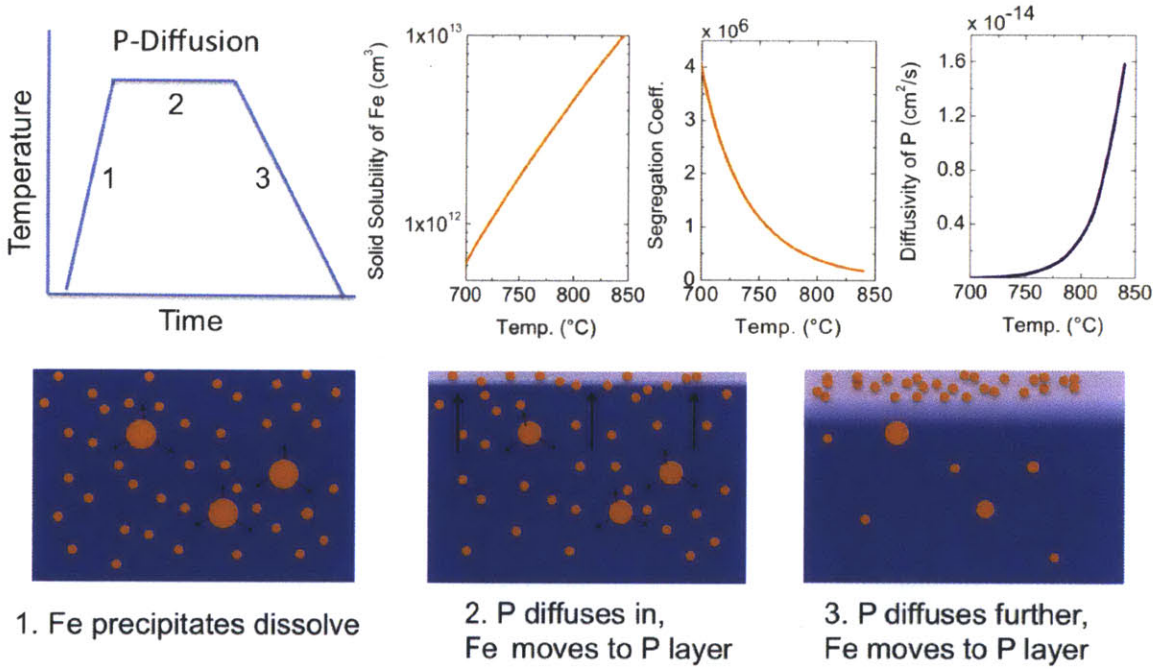


Figure 2-4: Phosphorus Diffusion Gettering Schematic (adapted from [23])

The mechanisms of gettering iron to a phosphorus-rich, n-type layer are still not definitively known, but there have been a few different hypotheses. In p-type silicon, interstitial iron is positively charged because the Fermi level is below the energy level of the iron impurity. The solubility of interstitial iron increases with the boron doping level because positively charged interstitial iron can pair with an increasing concentration of B^-. However, in n-type silicon, there is not a directly analogous effect in heavily phosphorus-doped silicon because interstitial iron is electrically neutral,

so it does not Coloumbically pair with positively charged substitutional phosphorus. Haarahiltunen *et al.* [22] proposed a semi-empirical two-reaction model based on Bentzen *et al.*'s assumption that phosphorus diffuses via vacancies when the phosphorus concentration is high [24]. Haarahiltunen *et al.* hypothesize that doubly negatively charged vacancies bond with neutral interstitial iron to produce negatively charged substitutional Fe_s^- and an electron, e^-. The negatively charged substitutional iron can then pair with positively charged ionized phosphorus. This pair of reactions is illustrated in Fig. 2-5. In response to this proposed model, Syre *et al.* [25] measured with secondary ion mass spectroscopy the concentrations of phosphorus, iron, and oxygen as a function of depth in phosphorus-diffused float zone silicon samples. They concluded that the phosphorus-rich layer produces vacancies, which are energetically favorable oxygen precipitation sites. At these clusters of vacancies and oxygen, there are sites for which iron gettering is favorable. Thus, although both theories describe the same net effect, the actual mechanism is still not definitively known.

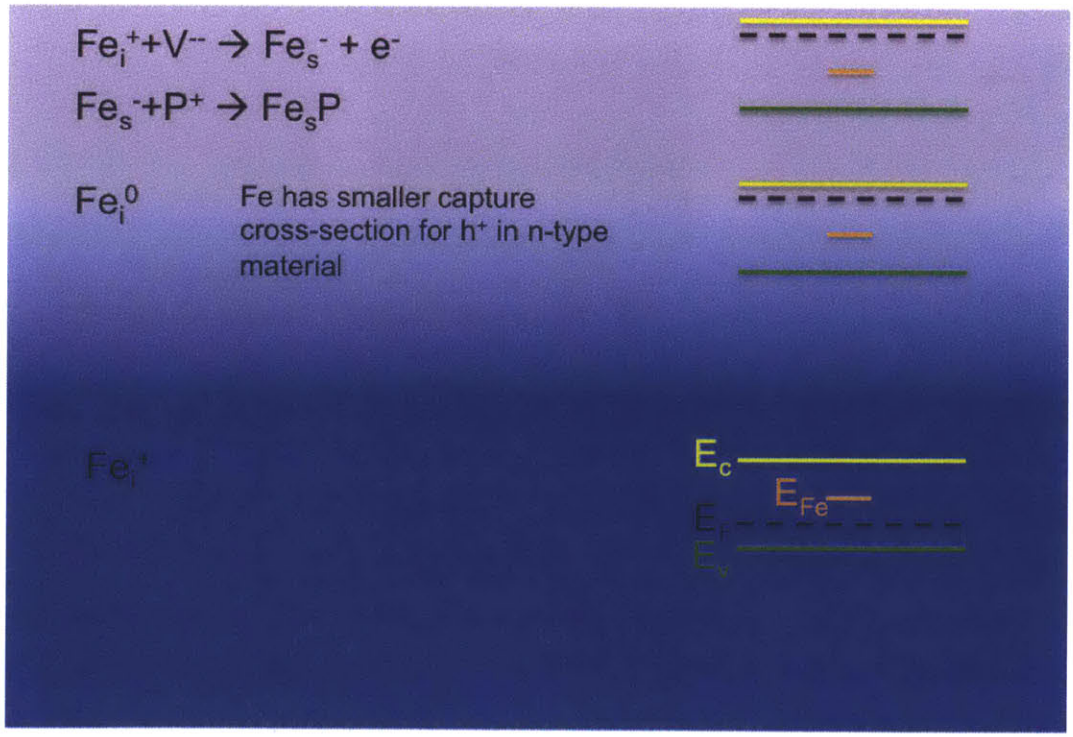


Figure 2-5: Mechanism of phosphorus diffusion gettering as proposed by Haarahiltunen *et al.* [22]

2.4 Review of Approaches to Optimizing the Phosphorus Diffusion Time-Temperature Profile for Gettering of Iron

As discussed above, a typical time-temperature profile of the phosphorus diffusion step consists of a ramp up to a high temperature, a hold at that high temperature during which phosphorus is thermally diffused from a surface boundary layer, followed by some cooling profile [26]. There have been a number of alternatives to this standard process with modeling and experimental support. Multiple authors [27, 28] have investigated rapid-thermal annealing from spin-on dopant sources, achieving cell efficiencies as high as 17.5% for high-purity Czochralski silicon. However, a reduction in cell performance was observed for materials with higher iron concentrations [29]. Plekhanov simulated gettering profiles for materials with higher iron concentrations, exploring higher temperatures to promote precipitate dissolution [30]. In subsequent years, Manshanden compared a single-step plateau profile to a two-step plateau profile and found that the two-step process is more effective at gettering iron point defects [31]; the physics of the process was clarified by subsequent work by Pickett [32] and Rinio [33] and related to the time-temperature transformation diagram of iron interstitials in silicon [11]. Schön explored a profile consisting of a ramping high-temperature pre-anneal followed by a plateau [34] similar to Plekhanov [30]. Ossiniy explored similar multi-plateau profiles designed to enhance precipitate dissolution and point-defect gettering, resulting in higher minority carrier lifetimes [35].

In this thesis, a phosphorus diffusion profile that incorporates many of the benefits of these previous approaches with the goal of optimizing for both manufacturing throughput (process time) and electrical performance is simulated and experimentally tested. As an alternative to a standard plateau profile, it is hypothesized that ramping up to a peak temperature above the typical process hold temperature and then immediately ramping down with no holding time could accelerate impurity gettering. It

is hypothesized that, while keeping sheet resistance constant, this continuously ramping process increases minority carrier lifetime while also shortening overall processing time for a range of initial iron concentrations.

Chapter 3

Impurity-to-Efficiency Simulator

The physics and the resulting device performance discussed above can be described in simulation, rendering solar cell processing predictable.

The model applied in this thesis, the Impurity-to-Efficiency (I2E) simulator is a one-dimensional solver currently running in MATLAB that focuses on the essential physics of phosphorus diffusion kinetics to enable the rapid testing of a wide processing parameter space [10, 36]. I2E points toward optimization of solar cell processing for a wide variety of input materials. It is schematically illustrated in Fig. 3-1. The inputs are the as-grown distribution of iron, the time-temperature profile of the processing, and the solar cell device architecture. The model then solves coupled partial differential equations describing phosphorus diffusion, iron diffusion, the segregation of interstitial iron to the phosphorus-diffused layer, and iron precipitate growth and dissolution. Based on the final distribution of iron, the final effective lifetime due to interstitial and precipitated iron is calculated. Finally, the profiles of lifetime and phosphorus as a function of depth can be input to *PC1D* to calculate a final solar cell efficiency [13]. Thus, the outputs are the phosphorus, precipitated iron, and interstitial iron concentrations, and minority carrier lifetime as a function of depth into the cell, and the final solar cell efficiency. This thesis focuses on characterizing and improving the material quality, so here the cell structure and solar cell efficiency will not be discussed further. Instead, the minority carrier lifetime will be the final measure of electrical quality because it is often positively correlated with solar cell

efficiency, assuming an optimized solar cell architecture.

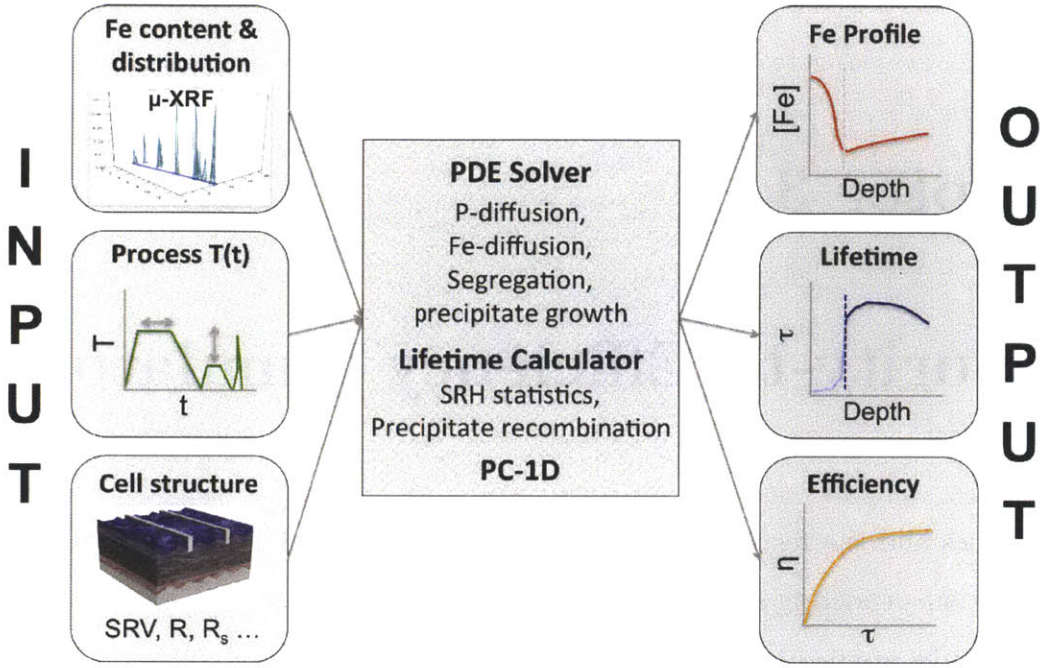


Figure 3-1: Diagram of Impurity-to-Efficiency simulation tool (reprinted from [37])

The inputs to I2E can be measured experimentally. The size and linear density of precipitates can be quantified with synchrotron-based X-ray fluorescence spectroscopy. Total iron concentration can be detected by inductively coupled plasma mass spectrometry (ICP-MS). Interstitial iron concentration can be measured with Quasi-Steady State Photoconductance. Any time-temperature profile can be tested, but there are engineering limits imposed by the furnaces used to process the wafers.

The phosphorus profile as a function of depth is described using Bentzen *et al.*'s model [24], and the segregation of iron to the phosphorus layer is modeled using Haarahiltunen *et al.*'s semi-empirical model [22]. Iron precipitate dissolution and growth is assumed to be well-described by Ham's law [38]. The lifetime of electrons in the boron-doped bulk is described by Shockley-Read-Hall statistics [16], and recombination due to precipitates is described by del Cañizo *et al.* [19]. The diffusion-segregation equation used to describe the concentration of interstitial iron as a function time due to diffusion and segregation to the emitter is from Tan *et al.* [39].

3.1 Solar Cell Process Design Principles from I2E

I2E is uniquely set up to rapidly solve a broad parameter space, allowing for the extraction of general design principles for an unconstrained maximization of the lifetime after the phosphorus diffusion step [21, 37, 40, 41]. For single crystalline, highly pure silicon materials, shorter, higher temperature isothermal steps provide adequate impurity gettering, achieve high sheet resistance for improved absorption of the blue end of the solar spectrum, and allow for faster manufacturing throughput. For less pure multicrystalline silicon materials, higher temperature, longer isothermal steps with a longer controlled cool are important to getter higher concentrations of impurities. However, this extended time and temperature approach sacrifices throughput and reduces the emitter sheet resistance.

3.2 Adding a Sheet Resistance Calculation

The sheet resistance of the phosphorus-diffused emitter layer is an important solar cell device parameter. Shallower emitters (high sheet resistance) improve the conversion of light from the blue end of the solar spectrum while deeper emitters (lower sheet resistance) reduce the risk of shunting the solar cell during contact deposition and firing. As process control and contact techniques improve, the PV industry is moving from 60-70 Ω/sq. toward higher sheet resistances of around 100 Ω/sq. [42]. Additionally, cell processes downstream of the phosphorus diffusion step are optimized for a given sheet resistance and phosphorus profile. The addition of a first-principles-based sheet resistance model to the I2E tool enables a constrained co-optimization of processing for sheet resistance and final minority carrier lifetime.

For a typical solar cell process, the sheet resistance is a function of the phosphorus concentration as a function of depth into the silicon wafer. As shown in Eq. 3.1, the sheet resistance is the inverse of the conductivity integrated over the thickness of the phosphorus layer.

$$R_{sh} = \frac{1}{\int_0^d \sigma(\mathrm{x})\,\mathrm{d}x} \tag{3.1}$$

As shown in Eq. 3.2, the conductivity as a function of depth into the wafer is the product of the charge carrier mobility as a function of depth into the wafer, the elementary charge, and the electrically active phosphorus concentration as a function of depth into the wafer. Throughout the I2E model, it is assumed that the electrically active phosphorus concentration and the electron concentration are equal.

$$\sigma(x) \;=\; \mu(x) q [P^+](x) \tag{3.2}$$

Klaassen's mobility model was used to compute the mobility of electrons and holes [43, 44]. The effect of band gap narrowing was neglected (an approximation leading to error in calculated sheet resistance of less than 0.2%). Additionally, the model does not consider the formation of the phosphosilicate glass on the surface of the silicon wafer during diffusion. With the addition of this sheet resistance model to the I2E simulator, it was possible to tune the phosphorus diffusion time-temperature profile to simultaneously achieve a certain target sheet resistance and maximize minority carrier lifetime in the bulk of the wafer without increasing processing time.

Chapter 4

Simulations of Standard and Continuously Ramping Phosphorus Diffusion Time-Temperture Profiles

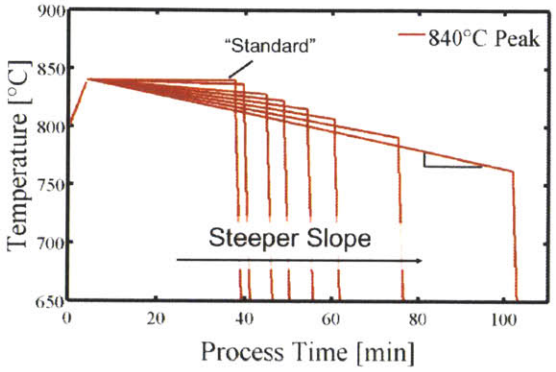
Understanding of the kinetics of phosphorus and iron during solar cell processing was combined with the I2E model to compare in simulation the effect of standard and continuously ramping phosphorus diffusion time temperature profiles on solar cell material quality. This simulation work is based on and updated from a manuscript presented at the 38th IEEE Photovoltaic Specialists Conference [45].

4.1 Defining the Time-Temperature Profiles

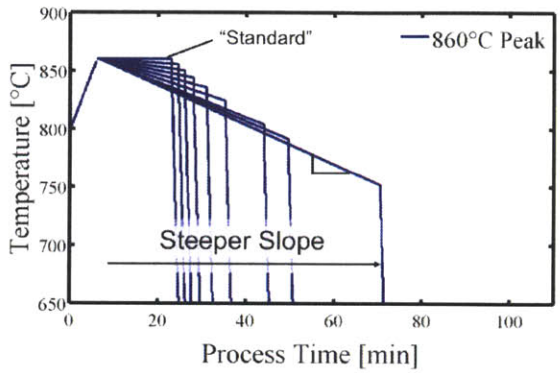
First, a standard phosphorus diffusion profile consisting of a ramp up from 800°C to a constant high-temperature plateau followed by an exponential cool from the high temperature plateau with an exponential time constant of 6 min, which is roughly equivalent to removing the wafer from the furnace to cool, was simulated. Phosphorus flow starts once the plateau temperature is reached.

As an alternative, a profile that moves from high temperature where precipitates

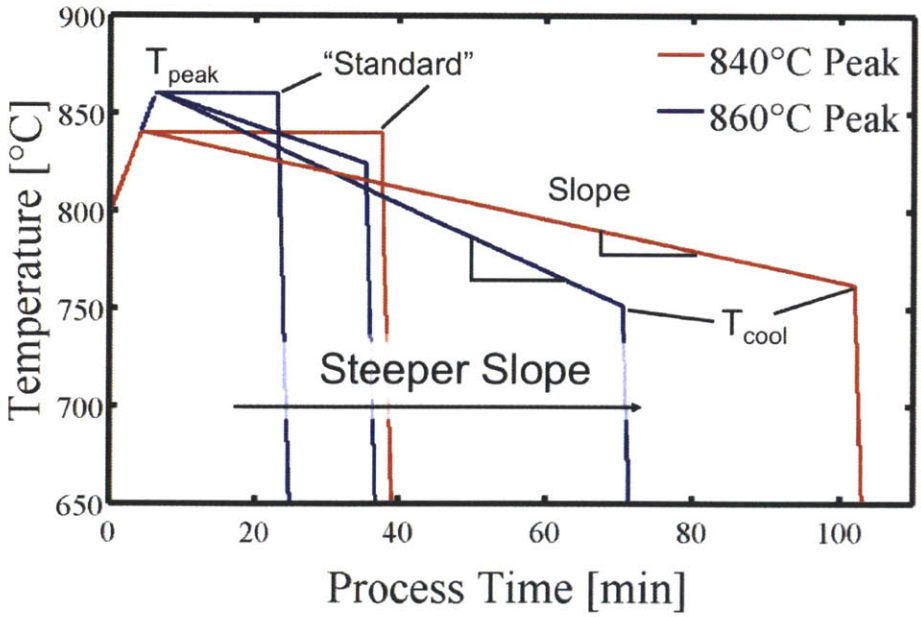
dissolve to lower temperature where iron point defects are strongly driven to the phosphorus layer was considered. The continuously ramping phosphorus diffusion profile consists of a ramp up from 800°C to a peak temperature, then a ramp down to a lower temperature with no hold time and an exponential cool with a 6 min time constant. In order to simulate experimentally testable time-temperature profiles, a linear controlled cool slope from the peak temperature was chosen. The phosphorus diffusion starts at the peak of the profile.



(a) T(t) profiles for 840°C maximum temperature



(b) T(t) profiles for 860°C maximum temperature



(c) A subset of T(t) Profiles for Comparison

Figure 4-1: Simulated 80 Ω/sq. Phosphorus Diffusion Time-Temperature Profiles

The simulated time-temperature profiles for two different maximum temperatures,

840°C, a typical process temperature and 860°C, a higher temperature, are shown in Fig. 4-1. Fig. 4-1(c) shows a selection of profiles from (a) and (b) for easier comparison. The parameters used for the simulations were typical for silicon solar cell material: surface concentration of phosphorus = 3×10^{20} cm^{-3}, initial interstitial iron concentration = 10^{11} cm^{-3}, initial total iron concentration = 10^{14} cm^{-3}, initial iron precipitate radius = 25 nm. For both standard and continuously ramping profiles, the sheet resistance was held constant at 80 Ω/sq., a typical or slightly high sheet resistance [42]. For each temperature, the standard profile is the one with the isothermal step and the shortest time because phosphorus diffuses in rapidly at high temperature. All of the profiles with continuously ramping temperatures (no isothermal steps) are variations of the alternative approach. For the 840°C maximum temperature, the slope of the controlled cool portion of the profile varied from 0°C/min (standard) to 0.8°C/min. For the 860°C maximum temperature, the slope of the controlled cool portion of the profile varied from 0°C/min (standard) to 1.7°C/min. For the standard profile, for each plateau temperature, the plateau time was adjusted until 80 Ω/sq. was achieved. For the continuously ramping profiles, for each pair of peak temperature and controlled cooling slope from the maximum temperature, the controlled cool time was adjusted until 80 Ω/sq.was achieved.

As the process temperature increases, the phosphorus diffusivity increases exponentially and therefore, the required process time to achieve a given sheet resistance decreases. Thus, for a higher target sheet resistance, shorter process times are required. For the continuously ramping profiles, a higher temperature allows access to both higher and lower temperature for a given process time and sheet resistance. Additionally, somewhat counterintuitively, a steeper controlled cool (further deviation from standard) results in longer process times because as the temperature decreases, the phosphorus diffuses in less rapidly.

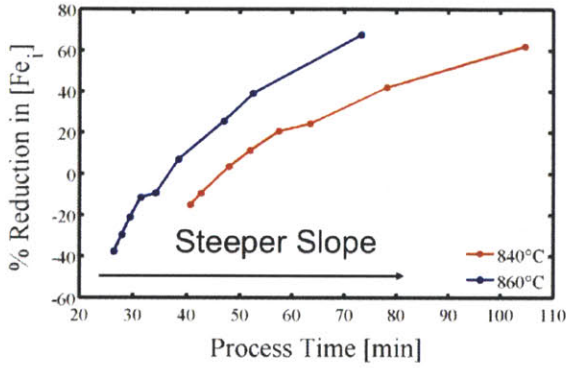
4.2 Calculated Effect of Standard and Continuously Ramping Phosphorus Diffusion Time - Temperature Profiles

The final iron distribution and resulting effective bulk lifetime for each of the time-temperature profiles shown above were simulated using I2E.

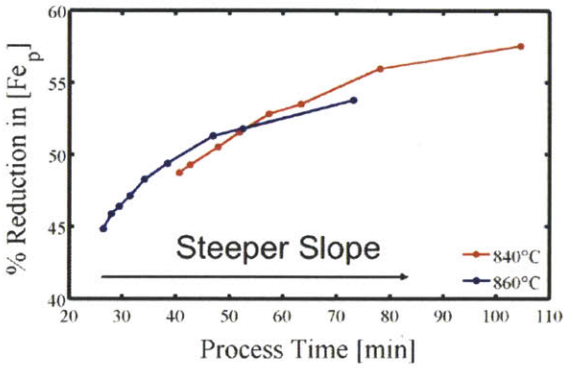
The percent reduction of interstitial iron due to processing for each of the simulated time-temperature profiles is shown in Fig. 4-2(a). Each of the points corresponds to one of the simulated time temperature profiles shown in Fig. 4-1(a) and (b). The simulation results indicate that for a given peak temperature, compared to the standard isothermal process, the longer processes with steeper ramping down slopes reduce iron point defects more effectively because the segregation coefficient, which is the driving force for iron to the phosphorus-rich layer, increases as temperature decreases, and the extra time is spent at high enough temperatures that iron can still diffuse through the silicon lattice relatively quickly.

The percent reduction in precipitated iron due to processing for each of the simulated time-temperature profiles is shown in Fig. 4-2(b). For a given peak temperature, profiles with steeper controlled cool slopes reduce precipitated iron concentrations more effectively. For these parameters and profiles, for processes less than 55 min, a higher peak temperature can reduce precipitated iron concentration more effectively in less time. For processes longer than 55 min, lower peak temperature dissolves iron precipitates more effectively because the wafers are at a higher temperature for longer. It is beneficial to reduce the concentration of precipitated iron as long as the process can segregate the resulting point defects to the phosphorus-rich layer.

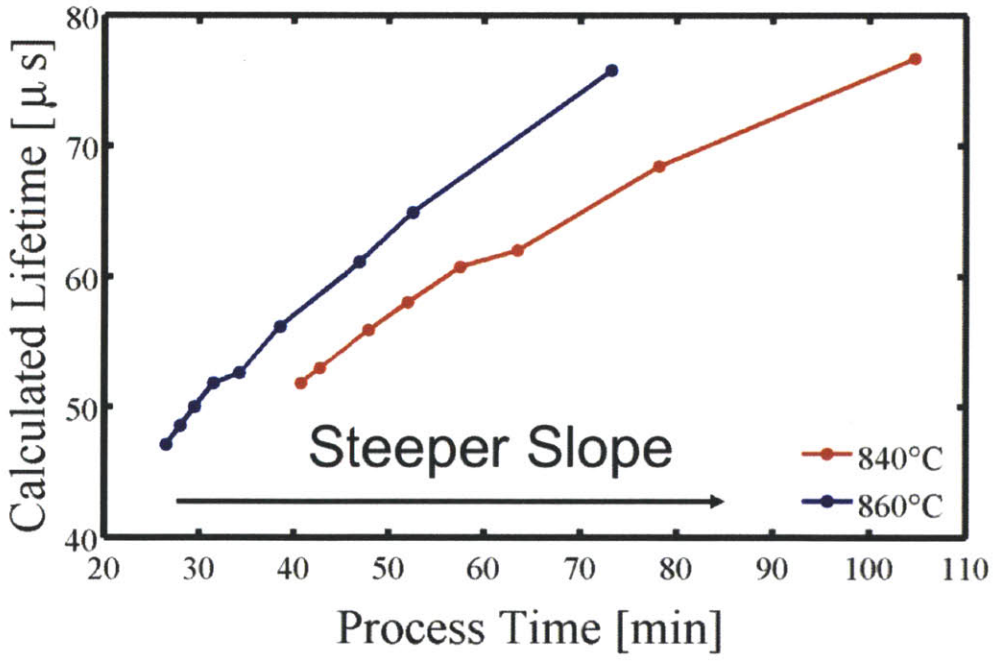
Consistent with the calculations of interstitial and precipitated iron concentrations, for a given peak temperature, steeper cooling slopes result in a higher effective lifetime. Additionally, higher maximum temperature processes can produce a higher effective lifetime in shorter time, as illustrated in Fig. 4-2(c). The simulated trends shown here hold for a wide parameter space relevant to solar cells.



(a) % Reduction in Interstitial Iron



(b) % Reduction in Precipitated Iron



(c) Calculated Lifetime After Processing

Figure 4-2: Continuously ramping profiles are predicted to improve iron reduction and increase lifetime

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Chapter 5

Silicon Samples and Experimental Methods

Two different silicon materials, monocrystalline and multicrystalline, were selected to experimentally compare the effect of a standard and an alternative phosphorus diffusion time-temperature profile on iron distribution and minority carrier lifetime. The multicrystalline silicon was etched to remove surface damage from sawing. Then, the resistivity and thickness of the samples were measured. Finally, the interstitial iron concentration, iron precipitate distribution, and minority carrier lifetime were measured before and after phosphorus diffusion processing.

5.1 Silicon Sample Selection

Silicon solar cell materials have a wide range of purity and defect levels. Thus, two different silicon materials were chosen based on their thickness and resistivity to experimentally test the effect of the simulated phosphorus diffusion profiles.

Representing relatively defect-free, pure material, eighteen wafers of two-inch diameter, 250-300 μm Czochralski-grown single-crystal, 1-10 Ω-cm <100> silicon (CZ-Si) were selected. One side was polished and the other side was etched by the wafer manufacturer. Each sample was labelled with a diamond-tipped scribe pen on the polished side.

On the other hand, eighteen samples of multicrystalline silicon (mc-Si) were selected to represent defect-rich, impure material. The ingot from which the samples were chosen was grown from the tops of 40 other standard industrial ingots. Two vertically adjacent wafers were chosen from 90% ingot height and then laser cut into nine two-inch wide samples for sheet resistance, lifetime, and interstitial iron concentration measurements and a few smaller samples for total iron concentration and precipitated iron studies. A sample set separate from that used to characterize the lifetime and interstitial iron was used because the sheet resistance and lifetime measurements require samples at least two inches in diameter, but the synchrotron beam line sample stage accommodates only small samples (up to about 1 cm^2), and typically, less than 1 mm^2 on each sample is scanned. Inductively coupled plasma mass spectrometry (ICP-MS), which is destructive and thus requires a dedicated sample, indicated that the total as-grown iron concentration of these wafers is 1.1×10^{15} cm^{-3}. All of the mc-Si samples are expected to have similar total iron concentration because they come from two vertically adjacent wafers, essentially the same ingot height. Samples from the same wafer have different defect structures. Thus, the most similar samples are those from the same position on two vertically adjacent wafers. These mc-Si samples were labelled with the laser during the sample cutting process.

Optical scans of the two materials are shown in Fig. 5-1. Fig. 5-1(a) shows the polished side of a two-inch CZ-Si wafer. Fig. 5-1(b) shows the nine two-inch samples cut from one of the vertically adjacent full-size mc-Si wafers. The visible variations of gray are differently oriented crystal grains typical of cast mc-Si silicon.

The samples described above were put through the following experimental procedure with careful attention to minimizing contamination during processing and reducing systematic error introduced by processing steps.

5.2 Saw Damage Etching Multicrystalline Silicon

The mc-Si wafers used in this experiment were sliced from an ingot with a sawing process, so the as-cut wafers have a surface layer of damaged silicon approximately

(a) 2" CZ sample

(b) 2" mcSi samples cut from one full wafer

Figure 5-1: Optical scans of silicon samples. (a) One of the two-inch CZ-Si samples. (b) Nine two-inch-wide mc-Si samples cut from one full mc-Si wafer

10 μm thick. This layer contains high concentrations of impurities from the sawing slurry, which can contaminate the wafer during processing. Additionally, the silicon in this surface layer is mechanically damaged, which can lead to wafer breakage during processing. Therefore, this layer is chemically removed with the following chemical process:

- Dip in hydrofluoric acid (HF) for at least 30 seconds to remove native oxide.
- CP4 chemical bath consisting of 70% nitric acid, 100% acetic acid, and 49% HF in a ratio of 15:5:2.
- Dip in HF to remove oxide that forms during CP4 etch.
- Bath of 30% by weight potassium hydroxide (KOH) dissolved in water at room temperature for 1 minute.
- Dip in HF to remove oxide that forms during KOH bath.

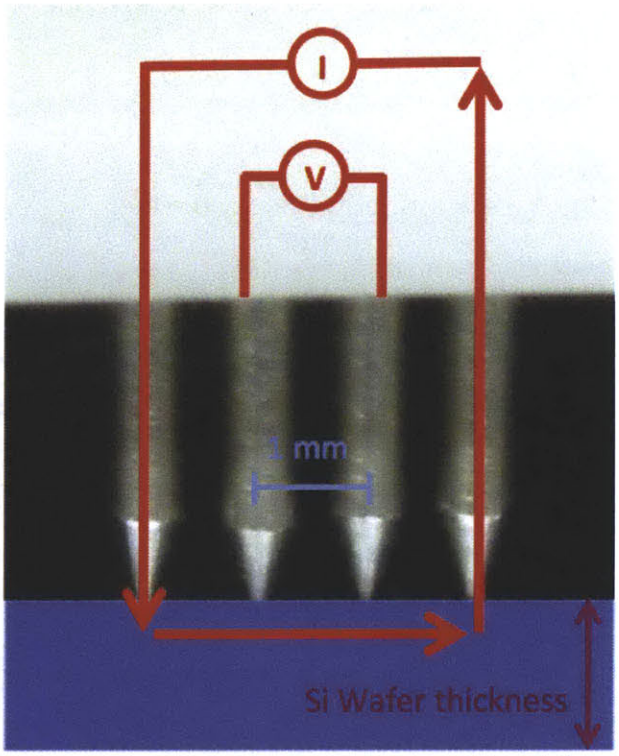
Before and after each HF dip, the samples were rinsed with deionized water. This etch results in a fairly uniform reduction in thickness with a slightly higher etch rate at the sample edges. The reaction is exothermic, and the etch rate increases with temperature and the surface area of silicon in the bath. To verify how much silicon was removed during the etching step, the wafer sample thickness was measured with a micrometer and the wafer mass was measured with a mass balance before and after etching. Assuming the facial area of the wafer remains the same, the average thickness of the wafer was calculated by multiplying the initial thickness, d_0, by the ratio of the post-etching mass, m_{etched}, and pre-etching, m_0 mass as in Eq. 5.1. The wafer thickness is also an input parameter for the resistivity and lifetime measurements and the I2E simulator.

$$d_{etched} = d_0 \frac{m_{etched}}{m_0} \tag{5.1}$$

5.3 Bulk Resistivity Measurement

In typical p-type wafers for solar cells, the bulk resistivity is determined by the boron concentration. In addition to being a key electrical property of the material, the resistivity is an input to the minority carrier lifetime measurement and to I2E. A standard four-point probe configuration, shown in Fig. 5-2, was used to measure the resistivity. Current is passed through the outer two probes, and a potential difference is thereby induced between the two inner probes. The resistance is given by the slope of the curve of the induced voltage plotted against the range of currents swept. The resistivity is the resistance divided by the wafer thickness. The appropriate driving current must be used to achieve accurate resistance and resistivity measurements [46]. Higher currents allow for a higher signal-to-noise ratio, but if the current is too high, charge carriers can be injected into the sample, leading to an erroneous measurement.

(a) Four Pt Probe Experimental Setup



(b) Four Pt. Probe Schematic (adapted from [47])

Figure 5-2: In a four-point probe configuration, current passes through the outer two probes and the sample, and the induced voltage is measured by the two inner probes. The probe spacing shown here is 1 mm.

5.4 Minority Carrier Lifetime Measurement

The minority carrier lifetime and the concentration of interstitial iron were measured before and after phosphorus diffusion. To reduce the recombination at the wafer surfaces, the surfaces are electrochemically passivated with aluminum oxide before the lifetime measurements [48].

1. Chemical Surface Clean in Preparation for Surface Passivation

   Before depositing the aluminum oxide, the wafer surfaces were chemically cleaned with an RCA clean [49] consisting of the following steps:

   - Dip in HF for at least 30 seconds to remove native oxide
   - Bath of 5:1:1 deionized water: ammonium hydroxide: hydrogen peroxide for 10 minutes at 70°C (RCA1)

- HF dip to remove RCA1 silicon oxide
- Bath of 5:1:1 deionized water : hydrochloric acid : hydrogen peroxide for 10 minutes at 70°C (RCA2)
- Rinse in deionized water

Before and after each HF dip, the samples were rinsed with deionized water. The oxide that forms during the RCA2 bath is not etched before aluminum oxide deposition because it has been shown that the passivation is more effective with a surface oxide present [50].

2. Atomic Layer Deposition of Aluminum Oxide for Surface Passivation

   After surface cleaning, aluminum oxide was deposited on both sides of each wafer via atomic layer deposition (ALD) using a S200 Savannah at Harvard University's Center for Nanoscale Systems (CNS). First, small silicon chips were placed in the chamber and 5 nm of Al_2O_3 were deposited at 200°C. Next, the samples were placed in the chamber, raised slightly above the chamber floor by the small silicon chips, and 20 nm of Al_2O_3 were deposited at 200°C [51]. To densify the film and activate the passivation, the wafers were annealed at 375°C for 12 minutes in nitrogen [48].

3. Minority Carrier Lifetime Measurement

   A tool for measuring the effective minority carrier lifetime of a silicon wafer without electrical contacts is the Sinton WCT-120 Photoconductance Lifetime Tester [52]. Minority carrier lifetime can be expressed as in Eq. 5.2 [53]. The lifetime depends on the excess minority carrier density, Δn, the carrier generation rate, G, and the derivative of the excess carrier density as a function of time.

$$\tau = \frac{\Delta n}{G - \frac{d\Delta n}{dt}} \tag{5.2}$$

There are two approximations that can be used to simplify the equation, one in

which the generation rate, G, is zero and one in which the excess carrier density, Δn, is in steady state, $\frac{\Delta n}{dt} = 0$. In each of the two following measurement modes, one of the two assumptions is fulfilled: transient photoconductance decay (PCD) and quasi-steady-state photoconductance (QSSPC).

In PCD, the sample is flashed with a fast light pulse that decays in 1020 μs. This fast flash results in a high concentration of excess carriers in the sample even after the flash has decayed. After the flash has terminated, the decaying conductivity of the silicon sample is measured as a function of time with the built-in radio frequency coil. During the measurement, no additional carriers are excited, so the generation rate, G, is zero. The excess carrier density as a function of time is calculated from the measured conductivity decay. The lifetime is then calculated using Eq. 5.3.

$$\tau = \frac{\Delta n}{-\frac{d\Delta n}{dt}} \tag{5.3}$$

The fast flash decays in 1020 μs, and the sample lifetime must be significantly longer than the flash decay time; thus, the PCD mode is valid for lifetimes greater than 100 μs.

On the other hand, in QSSPC mode, the sample is flashed with a light pulse that decays slowly, 12 ms. This slow flash results in a quasi-steady-state concentration of excess carriers as the flash decays. While the flash decays, the flash intensity is measured with a built-in light sensor near the sample, and the conductivity is measured as a function of time. As in PCD mode, the excess carrier density as a function of time is calculated from the measured conductivity. The generation rate is calculated from the light intensity reading and the user-provided optical constant, which estimates the fraction if incident light that is absorbed into the sample. The lifetime is then calculated using Eq. 5.4.

$$\tau = \frac{\Delta n}{G} \tag{5.4}$$

Because the flash decays in 12 ms, and the sample lifetime must be less than one tenth of the flash decay time; thus, the QSSPC mode is valid for lifetimes less than 200 μs.

To achieve an accurate measurement, it is important to calibrate the tool, enter the sample properties in the software, and use the appropriate filters and flash settings as described in the manual [52].

5.5 Interstitial Iron Concentration Calculation

Point defects in silicon that pair Coulombically with substitutional dopants can be measured with a contactless, non-destructive technique that is sensitive at less than parts per billion and even parts per trillion [54]. Iron in boron-doped silicon is one such defect. In the dark at room temperature, positively charged interstitial iron, Fe_i^+, combines with negatively charged substitutional boron, B_s^-, to form iron-boron pairs, Fe-B, as described by chemical Eq. 5.5.

$$Fe_i^+ + B_s^- \rightarrow FeB \tag{5.5}$$

Strong illumination breaks Fe-B pairs into interstitial iron and substitutional boron. The energy level and capture cross section of Fe_i^+ and Fe-B pairs are different, so the lifetime associated with each chemical state is different.

The effective lifetime, τ, when Fe-B pairs are dissociated can be expressed as the harmonic sum of the lifetime due to Fe-B pairs and other recombination pathways as expressed in Eq. 5.6. Similarly, the effective lifetime when Fe-B pairs are associated is expressed as in Eq. 5.7.

$$\frac{1}{\tau_{diss}} = \frac{1}{\tau_{Fe_i}} + \frac{1}{\tau_{diss,other}} \tag{5.6}$$

$$\frac{1}{\tau_{assoc}} = \frac{1}{\tau_{FeB}} + \frac{1}{\tau_{assoc,other}} \tag{5.7}$$

Assuming the lifetime due to non-iron defects is the same for the associated and the dissociated states, the difference in lifetime due to Fe-B pairs and the lifetime due to interstitial iron, Fe_i, can be calculated by measuring the lifetime when the iron is in each state as shown in Eq. 5.8.

$$\frac{1}{\tau_{Fe_i}} - \frac{1}{\tau_{FeB}} = \frac{1}{\tau_{diss}} - \frac{1}{\tau_{assoc}} \tag{5.8}$$

The concentration of Fe_i can be calculated from expression 5.9, where C is a function of the doping level, excess carrier density, and the fraction of Fe-B pairs that are associated [54, 55].

$$[Fe_i] = C(\frac{1}{\tau_{Fe_i}} - \frac{1}{\tau_{FeB}}) \tag{5.9}$$

Accordingly, two lifetime measurements were taken. First, the samples were flashed fifteen times with a 10-sun flash lamp to dissociate Fe-B pairs. Then lifetime was measured. The samples were then left in the dark until the Fe-B pairs reassociated at which time the lifetime was remeasured. The association time constant, τ_{assoc}, given by Eq. 5.10, depends on the bulk doping concentration, N_A, and the temperature, T [56]. For the CZ-Si, the association time was 7.5 hours and the doping concentration was 3.7×10^{15} cm^{-3}. For the mc-Si, the association time was 1.25 hours and the doping concentration was 2.65×10^{16} cm^{-3}.

$$\tau_{assoc} = 5 \times 10^5 \frac{T}{N_A} exp(\frac{0.66eV}{k_B T}) \tag{5.10}$$

5.6 Phosphorus Diffusion

After the as-grown samples have been characterized as described above, the aluminum oxide is removed with hydrofluoric acid, and the samples are RCA cleaned as described in section 5.4, with the addition of a final hydrofluoric acid dip right before loading into the phosphorus diffusion furnace.

A typical recipe consists of the following components: load wafers, heat wafers to

the phosphorus diffusion temperature, diffuse phosphorus into the silicon at that high temperature, allow the phosphorus to soak into the wafers while flowing nitrogen and oxygen, purge the furnace with oxygen, cool and unload the wafers. The phosphorus oxychloride bubbler temperature, gas flow rates, furnace size and geometry, and the history of processing carried out in the furnace are all factors that affect the result of the phosphorus diffusion process. However, in this experiment, the time-temperature profile was the focus.

The orientation of the two sets of wafers was designed to maximize the uniformity of the flow. The samples were placed vertically to active a double-sided diffusion. Several dummy wafers were placed in the outermost slots, then the CZ-Si test wafers were split into two groups and were placed just inward of the dummy wafers, and finally the mc-Si wafers were placed in the middle.

5.7 Sheet Resistance Measurement

After the phosphorus diffusion step, the sheet resistance of the phosphorus-diffused layer is measured with a four-point probe setup as described in section 5.3 with the appropriate driving current range. For the measurements performed for this experiment, the phosphosilicate glass (PSG) that forms during phosphorus in-diffusion was not etched. Typically, the presence of the PSG does not affect the sheet resistance measurement because the probe tips penetrate through the PSG to contact the phosphorus-diffused silicon below. There is usually variation across the wafer faces and between the fronts and backs of the wafers due to heterogeneity in the gas flows. Additionally, the sheet resistances measured on CZ-Si are typically higher than that of the mc-Si because phosphorus preferentially diffuses along grain boundaries more rapidly [57]. Accordingly, to characterize the average and standard deviation of the sheet resistance, each wafer was measured on both sides in three different locations.

Finally, the phosphorus-diffused emitter layer was chemically etched with CP4, and the sample thickness, the lifetime, and the interstitial iron concentration were remeasured as described above.

5.8 Characterizing the Distribution of Precipitated Iron with Synchrotron-Based micro-X-Ray Fluorescence

In parallel with the measurements of minority carrier lifetime and iron point defects described above, iron precipitates in two samples of the mc-Si material were measured with synchrotron-based micro-X-ray fluorescence spectroscopy (μ-XRF). From each of the two vertically adjacent wafers from which the eighteen larger samples originated, one sample was selected from the same sample position. The total iron concentration of both synchrotron samples was assumed to also be 1.1×10^{15} cm^{-3} as was measured by ICP-MS on a different sample from the same wafer.

After the samples were laser cut from the full size wafer, they were saw damage etched with CP4 and RCA cleaned. Then the as-grown precipitated iron distribution was measured at the synchrotron at a random angle grain boundary. Typically, high misorientation grain boundaries are measured because they are favorable heterogenous nucleation sites for metallic precipitates [57]. Additionally, scanning grain boundaries instead of intragranular regions ensures that the unique, exact location of the scan is known. Electron backscatter diffraction (EBSD) is used to characterize the grain structure and grain boundary type of the samples [58]. A sample that was in a third vertically adjacent wafer from the same horizontal position was polished, and grain orientations and grain boundary types were determined by EBSD. The samples were then RCA cleaned again and phosphorus diffused. Samples were processed vertically in a custom-made quartz try to achieve a double-sided diffusion for better comparability with the larger samples that were used for lifetime and interstitial iron measurements. The phosphosilicate glass that forms during phosphorus diffusion was removed with hydrofluoric acid. Finally, both samples were returned to the synchrotron, and the exact same region was measured again, allowing for a direct comparison before and after processing.

X-ray fluorescence spectroscopy is a characterization technique in which a material

is exposed to short wavelength, high-energy X-rays, causing the material to emit secondary photons. Incident photons with energy greater than the ionization energy of the given material can eject tightly held core electrons from the inner orbitals of the material. Electrons in outer orbitals then move to the vacated inner orbitals to stabilize the atom. To conserve energy, as the electrons transition from the outer to the inner orbital, they release photons with energy equal to the difference in energy between the outer and inner orbitals. This absorption of energy resulting in the emission of radiation of a different energy is called fluorescence. Detected elements can be differentiated from each other because each element has distinct characteristic magnitudes of energy difference between the orbitals [59, 60].

X-rays from a synchrotron light source are radiation from electrons being accelerated at nearly the speed of light in a circular path. Synchrotrons can produce high-energy, high-brilliance, high flux, very focused beams of photons. The measurements for this experiment were done using a 10 keV X-ray beam with a 200 nm spot size at beamline 2-ID-D at Argonne National Laboratory's Advanced Photon Source synchrotron facility. A sample stage with six degrees of freedom allows for high-resolution mapping of multiple elements simultaneously at minimum concentrations of 10^{14} atoms/cm^2. This high sensitivity enables the detection of metallic precipitates in mc-Si for solar cells [14]. Further detailed specifications for this beam line are available on the website of Argonne National Laboratory's Advanced Photon Source [59] and in David Fenning's Ph.D. thesis [21]. The data quantification procedure applied in this thesis is also detailed in Fenning's thesis.

Chapter 6

Experimental Results

To compare the effect of a standard and an alternative phosphorus diffusion process on silicon solar cell material electrical quality, the minority carrier lifetime and iron distribution for each sample were measured before and after processing.

6.1 Silicon Wafer Thickness and Resistivity

First, the thickness and resistivity of each wafer were measured before processing. These parameters are inputs to the minority carrier lifetime measurement, the interstitial iron concentration calculation, and the I2E simulations. The data are summarized in Table 6.1.

The measured monocrystalline silicon (CZ-Si) wafer thickness of 288 μm is within the manufacturer's range of 250-300 μm. The thickness of the multicrystalline silicon (mc-Si) wafers was measured after the saw damage etch.The mc-Si wafer thickness of 166 μm is reasonable as the wafers were cut from the ingot in 200 μm-thick wafers, i.e. about 34 μm were removed during the saw damage etch. The mc-Si wafer thickness is 60% of that of the CZ-Si. The standard deviation of the thickness, which was measured at the center of each wafer, for both materials was within 2% of the average value.

The driving current for the CZ-Si resistivity was 0.4 mA and that for the mc-Si resistivity was 2 mA [46]. The CZ-Si resistivity is within the manufacturer's 1-10 Ω-

cm rating while the mc-Si 0.6 Ω-cm is consistent with previous experimental results on the ingot [21]. The mc-Si bulk resistivity is about 16% that of the CZ wafers. The standard deviation of the resistivity, which was measured on each wafer in the center of the CZ-Si and in a large grain on the mc-Si, for both materials is less than 3.5% of the average.

Table 6.1: Sample Thickness and Resistivity

	thickness (μm)	resistivity (Ω-cm)
CZ-Si	288±6	3.8±0.05
mc-Si	166±3	0.6±0.02

6.2 Phosphorus Diffusion Time-Temperature Profiles

To assess if a continuously ramping phosphorus diffusion time-temperature profile produces a higher lifetime than a standard process, a pair of standard and continuously ramping time-temperature profiles was designed and implemented. The time temperature profiles measured by the furnace thermocouples are shown in Fig. 6-1. The blue curve is the standard process, and the red curve is the alternative continuously ramping one. Guided by simulations, the profiles were iteratively tuned to both have the same total process time and produce similar sheet resistances.

The initial fluctuation in temperature can be attributed to the exposing of the furnace to room temperature during the loading process. For both processes, the furnace is first heated to 800°C, at which point the processing begins. The standard phosphorus diffusion profile consists of a linear heating from 800°C to 824°C at 9°C/min followed by a 35-minute isothermal hold at 824°C during which phosphorus is diffused into the samples. The continuously ramping phosphorus diffusion profile consists of an linear heating from 800°C to 882°C at 9°C/min followed by a 30-minute linear cool at a rate of 3.1°C/min to 789°C during which phosphorus is diffused into the samples. For both processes, the samples are cooled in air by opening the furnace.

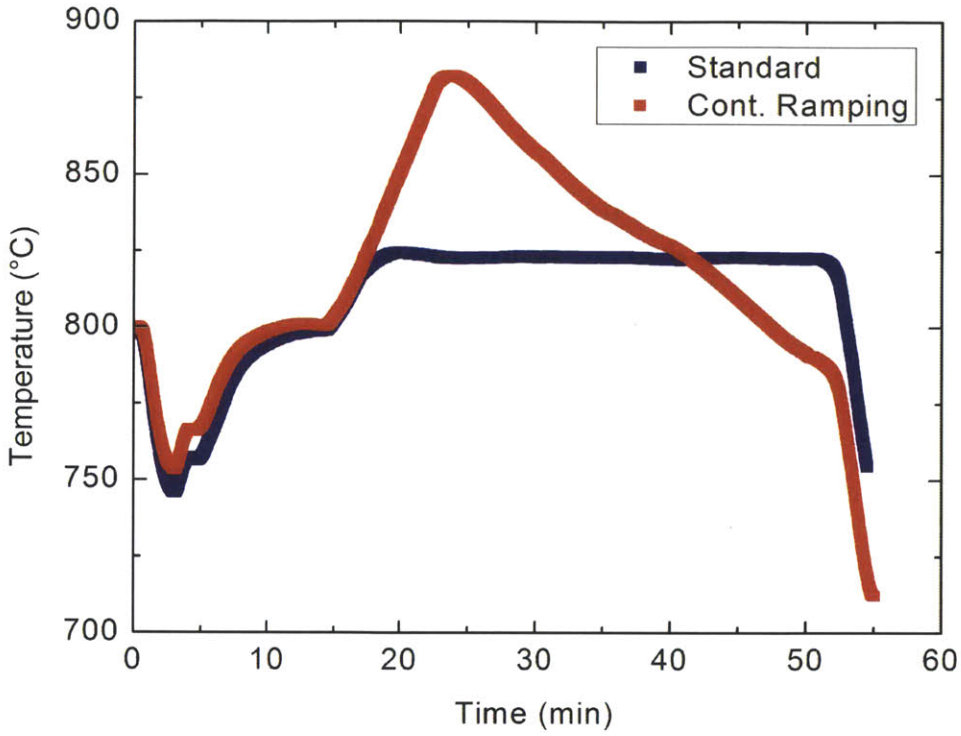


Figure 6-1: The pair of phosphorus diffusion time-temperatures profiles measured by the diffusion furnace thermocouples. The furnace was opened at 0 min. The samples were loaded within the first 5 min, and the furnace was opened at approximately 52 min.

Finally, both processes are 37 min long from the 800°C collected temperature state to the opening of the furnace.

6.3 Sheet Resistance Measurements

To check if the two processes produce similar sheet resistances, after phosphorus diffusion, the sheet resistance was measured in three different spots on both faces of each sample. The measurements are summarized in the column labelled R_{4pp} in Table 6.2. The average sheet resistances measured on the CZ-Si were higher than those of the mc-Si for both profiles, and the standard deviation of the sheet resistance was lower for CZ-Si than that of mc-Si. Both of these trends are expected because phosphorus diffuses preferentially along the grain boundaries and dislocations found in mc-Si, and the heterogeneity of mc-Si facets results in a more heterogeneous sheet

resistance [57].

Table 6.2: Measured and Simulated Sheet Resistance

Si Type	T(t) Profile	R_{4pp} ($\Omega/sq.$)	R_{sim} ($\Omega/sq.$)	$[P_{surf}]$ (cm^{-3})
CZ-Si	Standard	87.3 ±4.4	87	3.5×10^{20}
	Cont. Ramping	95.2 ±5.4	93.9	2.5×10^{20}
mc-Si	Standard	70.2 ±16.5	70.3	4.2×10^{20}
	Cont. Ramping	65.8 ±13.5	65.9	3.4×10^{20}

The difference between the averages of the mc-Si for the two different T(t) profiles is not statistically significant according to a two-tailed student's t-test with a p-value of 0.14. The difference between the averages of the CZ-Si for the two different time-temperature profiles is statistically significant according to a two-tailed student's t-test with a p-value of 3×10^{-13}, but the averages are within 10% of each other.

Using the phosphorus diffusion time-temperature profiles shown in the previous section, the emitter sheet resistance was simulated. The concentration of phosphorus at the surface of the wafer is assumed to be constant and is a fit parameter that is adjusted until the simulated and measured sheet resistances match. The simulated sheet resistance, denoted R_{sim} and the value of the fit parameter, $[P_{surf}]$, are also shown in Table 6.2. The values of the phosphorus surface concentration are within the range that has been measured with secondary ion mass spectroscopy [61].

After the sheet resistance was measured, in order to isolate the bulk of the silicon wafers for interstitial iron concentration and lifetime measurements, the phosphorus-rich emitter was etched off with CP4. The CZ-Si was etched for 3 min, reducing the thickness by 16 μm from 288 μm to 272 μm, while the mc-Si was etched for 2.5 min, reducing the thickness by 12 μm from 166 to 154 μm. This is expected to be more than sufficient to remove the emitter because none of the simulated p-n junction depths exceeded 1 μm.

6.4 Minority Carrier Lifetime and Interstitial Iron Concentration Measurements

To compare the effect of standard and alternative phosphorus diffusion profiles, the minority carrier lifetime and interstitial iron concentration of the samples were measured before and after processing as described in the previous chapter.

The as-grown data are summarized in Table 6.3. The CZ-Si samples were measured at an excess carrier density of $\Delta n = 8{\times}10^{15}$ cm^{-3} while the mc-Si was measured at $\Delta n = 4{\times}10^{15}$ cm^{-3}. The lifetimes reported here are when iron-boron pairs are associated. As expected, the lifetime, τ, of the purer, less defect-rich CZ was greater than that of the mc-Si. The standard deviations for both materials are within 10% of the mean value. Consistent with the lifetime data, the as-grown interstitial iron concentration, [Fe$_i$], of the mc-Si is greater than that of the CZ-Si with the standard deviation within 15% of the mean value.

Table 6.3: As-Grown Lifetime and Interstitial Iron Concentration Measurements

	Δn (cm^{-3})	$\tau_{FeB}(\mu s)$	[Fe$_i$] (cm^{-3})
mono-Si	$8{\times}10^{15}$	72.6 ±6.3	2.8±0.4 × 10^{11}
mc-Si	$4{\times}10^{15}$	17.1 ±1.3	9.1±0.7 × 10^{11}

Table 6.4: Phosphorus-Diffused Lifetime and Interstitial Iron Concentration

	$\tau(\mu s)$	[Fe$_i$] (cm^{-3})	τ_{sim}	[Fe$_i$]$_{sim}$	$\tau_{sim,lim}$
CZ Std.	457 ±153	5.9 ±3.3 × 10^{10}	116	$6.1{\times}10^{10}$	498
CZ Alt.	527±217	5.6±4.4 × 10^{10}	151	$3.8{\times}10^{10}$	533
mc-Si Std.	87.4 ±12.7	4.6±1.7 × 10^{10}	9.1	$1.8{\times}10^{10}$	308
mc-Si Alt.	87 ±11.9	4.7 ±1.4 × 10^{10}	12.8	$1.7{\times}10^{10}$	310

The measured lifetimes and interstitial iron concentrations after phosphorus diffusion are summarized in Table 6.4. For both processes and both materials, the lifetime is higher and the interstitial iron concentration is lower after processing. Interestingly, the standard deviations of the lifetime and interstitial iron concentration measurements were higher for the CZ-Si than for the mc-Si. For both materials, the processes

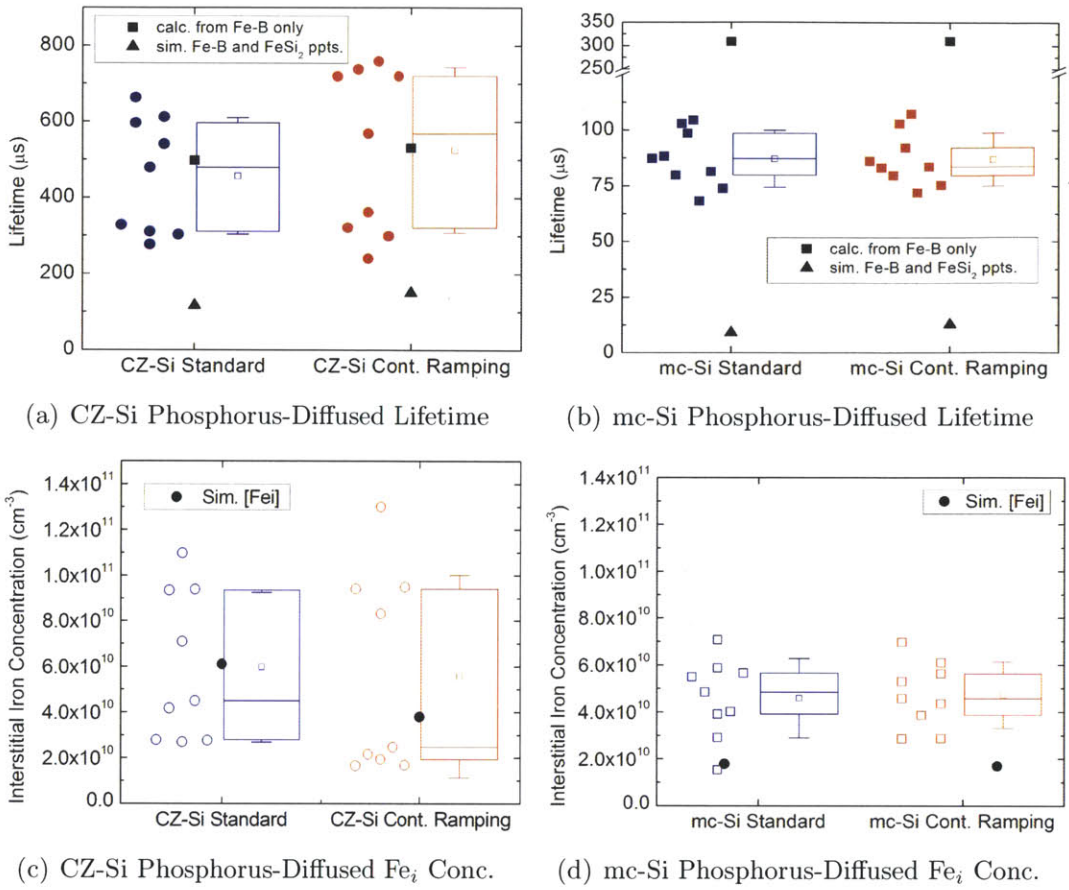
do not produce statistically different lifetimes or interstitial iron concentrations (student's t-test, two-tailed, p-values: CZ-Si [Fe_i] 0.83, CZ-Si lifetime 0.45, mc-Si [Fe_i] 0.86, mc-Si lifetime 0.96). Finally, although the lifetime of the CZ wafers was greater than that of the mc-Si, the interstitial iron concentration of the CZ-Si also was greater than that of the mc-Si. This trend has been seen in previous experiments, and it is likely due to internal gettering of interstitial iron to precipitates in mc-Si [21].

Fig. 6-2(a) and (b) summarize the minority carrier lifetime, τ, data. The lifetime of the CZ-Si samples processed with the standard profile have a mean of 458 μs and a standard deviation that is 33% of the mean. The lifetime of the CZ-Si samples processed with the continuously ramping profile have a higher mean of 527 μs and a wider standard deviation of 41% of the mean. On the other hand, the lifetime of the mc-Si samples processed with the standard profile have a mean of 87.4 μs and a standard deviation of 14.5% of the mean. The average lifetime of the mc-Si samples processed with the continuously ramping profile is 87.1 μs with a standard deviation that is 13.7% of the mean. In summary, the characteristics of the mc-Si were more similar than those of the CZ-Si for the two processes. Additionally, the standard deviations for the CZ-Si were greater than those of the mc-Si.

Fig. 6-2(c) and (d) summarize the interstitial iron concentration, [Fe_i], data. The [Fe_i] of the CZ-Si samples processed with the standard profile have a mean of 5.9×10^{10} cm^{-3} and a standard deviation that is 55% of the mean. The [Fe_i] of the CZ-Si samples processed with the continuously ramping profile have a lower mean of 5.6×10^{10} cm^{-3} and a larger standard deviation that is 80% of the mean. On the other hand, the [Fe_i] of the mc-Si samples processed with the standard profile have a mean of 4.6×10^{10} cm^{-3} and a standard deviation that is 36.7% of the mean. The average [Fe_i] of the mc-Si samples processed with the continuously ramping profile is 4.7×10^{10} cm^{-3} with a standard deviation that is 29.8% of the mean.

Overall, the CZ-Si started out, percentage-wise, with a wider range of lifetimes and interstitial iron concentrations and that trend persists after processing.

This pair of processes was also simulated using the Impurity-to-Efficiency simulator, and the simulated results are also plotted in Fig. 6-2. For the CZ-Si samples,



(a) CZ-Si Phosphorus-Diffused Lifetime

(b) mc-Si Phosphorus-Diffused Lifetime

(c) CZ-Si Phosphorus-Diffused Fe_i Conc.

(d) mc-Si Phosphorus-Diffused Fe_i Conc.

Figure 6-2: Measurements of post-processing minority carrier lifetime and interstitial iron concentration. The open square is the mean. The top and bottom edge of the boxes mark the first and third quartile, and the middle line is at the median value. The whiskers are at plus and minus one standard deviation.

the as-grown total iron concentration and initial average iron precipitate radius are unknown and are used as fit parameters. The total as-grown iron concentration was assumed to be 5×10^{13} cm^{-3}, a typical order of magnitude for CZ-Si, and the initial iron precipitate radius, was set to 25 nm because at this radius, the experimental and simulated interstitial iron concentrations matched well. The simulated results predict that the continuously ramping profile results in a higher lifetime (black triangles in 6-2(a) and (b)), and a lower interstitial iron concentration (black circles in 6-2(c) and (d)) for both materials. The simulated [Fe_i] better predicts the trends of the CZ-Si than the mc-Si because because the model assumes a homogeneous distribution of iron precipitates, thereby overestimating the effect of internal gettering of iron interstitials

to precipitates. For the same reason, for both materials, the model overestimates the negative impact of iron precipitates, so the lifetime is significantly underestimated. Simulations predict that for the CZ-Si, the continuously ramping profile results in $[Fe_i]$ that is 40% less than that of the standard profile while for mc-Si, the difference is only 5.5%. Multicrystalline silicon benefits from internal gettering to precipitates during both processes, so the additional benefit of a large segregation coefficient during the continuously ramping profile does not make as big a difference in the final interstitial iron concentration of the mc-Si as it does in the CZ-Si.

Finally, to gain insight into what defect might limit the lifetime of the material, the Fe-B pair limited lifetime (black squares in Fig. 6-2 (a) and (b)) was calculated using the average of the measured final interstitial iron concentration for each material. The CZ-Si is within 10% of its Fe-B-limited lifetime while the mc-Si is only 28% of its Fe-B-limited lifetime, indicating that the CZ-Si may be limited by iron point defects while mc-Si may be limited by metallic precipitates, dislocations, or some other recombination mechanism.

6.5 Iron Precipitate Distribution Measurements

The precipitated iron distributions of two samples, one for each time-temperature profile, were measured before and after processing using μ-XRF with 10 keV photons at beamline 2-ID-D at Argonne National Lab's Advanced Photon Source.

On the CZ-Si wafers dedicated to sheet resistance measurements that were processed with the synchrotron samples, the standard process resulted in sheet resistance of 76±2 Ω/sq. and the continuously ramping one resulted in 77±7 Ω/sq. These sheet resistance values are about 12% lower than those of the larger samples due to run-to-run process variability. Because the sheet resistances on the CZ-Si wafers were similar, it was assumed that the sheet resistances of the two synchrotron samples were similar to each other, making them comparable for this study.

The same region of interest on both samples at a random angle grain boundary with 33° misorientation was chosen from electron backscatter diffraction (EBSD)

maps, and it was identified as highly recombination active from micro-photoluminescence imaging at Fraunhofer ISE [62]. Shown in Fig. 6-3, high-resolution μ-XRF maps of the region were 18 μm high by 25 μm wide with 0.22 μm step size. 99% of the data were included for the fit of the background noise, and 3.5 standard deviations was used as the upper noise limit for the fit of a left-truncated normal distribution to the background noise. The background level was removed from the raw data. See Fenning's thesis for further details about quantifying the μ-XRF data [21].

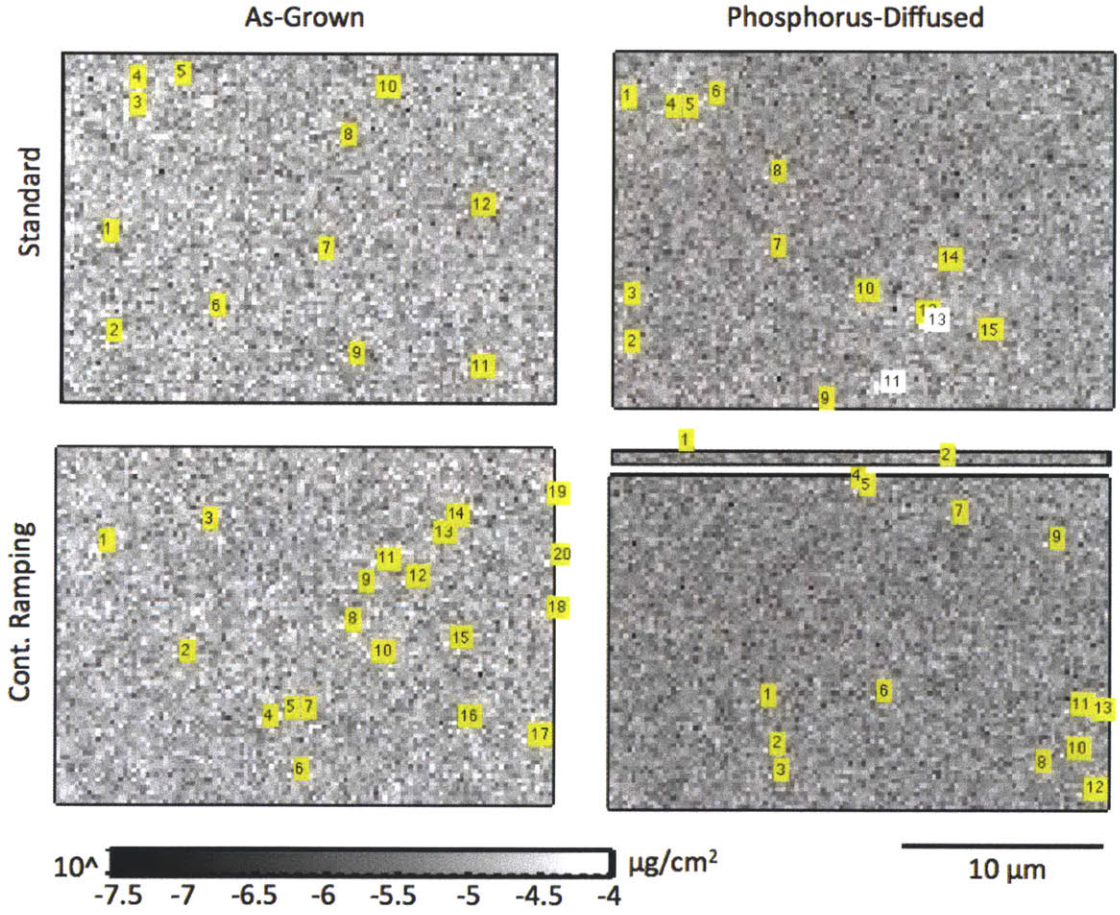


Figure 6-3: μ-XRF maps of iron before (as-grown) and after (Phosphorus-Diffused) processing for a standard and continuously-ramping phosphorus diffusion time-temperature profile. The yellow numbered labels are to the right of and slightly above the identified particles.

As shown in Fig. 6-3, it is very difficult to distinguish iron particles before and after processing for both phosphorus diffusion profiles, and the locations where the data quantification process identified iron particles before and after processing do

Table 6.5: Iron Precipitate Radii in mc-Si samples Before and After Processing

	T(t) Profile	Fe Ppt. Radius (nm)	Num. Ppts
As-Grown	Standard.	8.1 ±0.1	12
	Cont. Ramping	8.1 ±0.1	20
P-Diffused	Standard	7.7 ±0.6	15
	Cont. Ramping	7.4 ±0.2	15

not coincide. Additionally, for the standard process, more iron particles were identified after phosphorus diffusion than were identified before processing. These counts identified as iron particles may be an artifact of data processing and may not be actual precipitates. Thus, from these maps, it is not clear what the effect of either the standard or the continuously ramping profile is on the iron distribution, and no definitive conclusion about one profile more effectively reducing the concentration of precipitates can be drawn.

Nonetheless, to gain more insight, a statistical analysis of the sizes of the particles identified was done, and the data are summarized in Table 6.5 and Fig. 6-4. All the values are within 40% of the detection limit, which is about 7 nm radius precipitates, so it is difficult to know if the identified particles are real. Before processing, twelve iron precipitates were identified in the sample that was later processed in the standard process while twenty precipitates were identified in the sample later processed with the continuously ramping profile. Both samples had precipitates with an average radius of 8.1 nm with a standard deviation of 0.1 nm. After processing, fifteen iron precipitates were detected in each sample, three more particles than the number that were detected in the as-grown standard process sample. For both treatments, the average radii of the detected precipitates was lower and the standard deviation was higher after processing.

The difference between the average radius of precipitates in the sample processed in the continuously ramping profile and that of the sample processed with the standard profile is not statistically significant (student's t-test, p-value 0.065, two-tailed). Simulations predict that after processing, the precipitated iron concentration is 3.2×10^{14} cm^{-3} for the standard process and 1.5×10^{14} cm^{-3} for the continuously

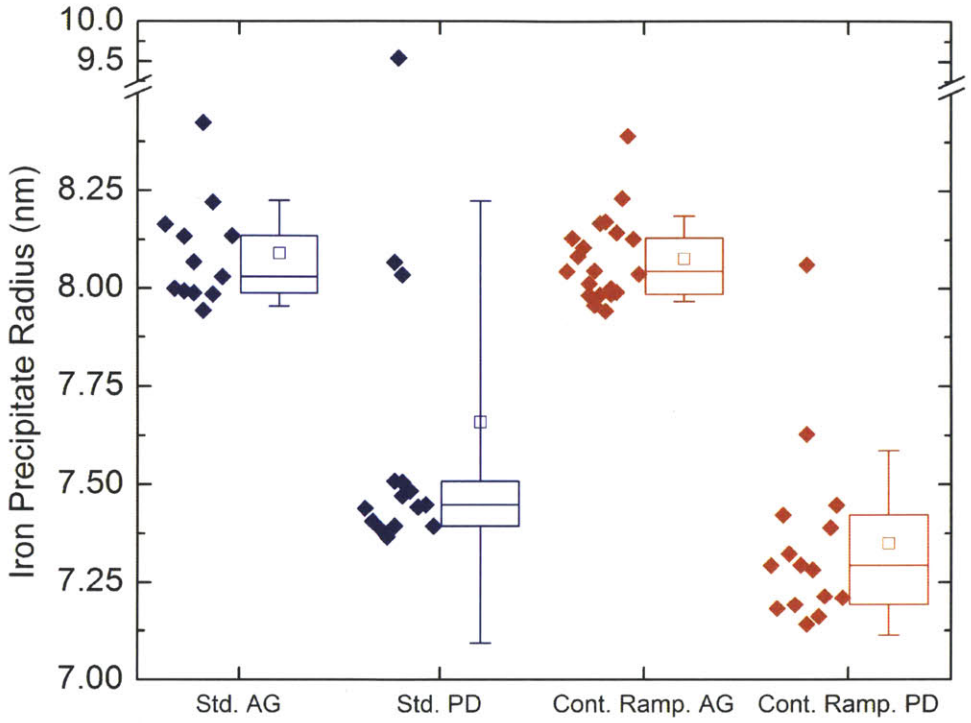


Figure 6-4: Apparent radius of iron precipitates before (AG) and after (PD) processing for a standard (std.) and continuously-ramping (Cont. Ramp.) phosphorus diffusion time-temperature profile

ramping process. These simulation results are consistent with the precipitate behavior observed by Fenning and Zuchlag *et al.* [63]. Although a stronger reduction of iron precipitates was expected for the alternative process, from these measurements, it is not possible to conclude that the higher temperature continuously ramping process more effectively dissolves iron precipitates than the standard process. That said, these data do not contradict the predictions from the simulations described in Section 4.2. Samples with higher initial iron precipitate concentrations may more definitively show the effect of each of the processes.

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Chapter 7

Discussion

The effect of two different phosphorus diffusion time-temperature profiles on the minority carrier lifetime and iron distribution of silicon wafers for solar cells was tested. The standard and the alternative continuously ramping phosphorus diffusion time-temperature profiles produce similar sheet resistances and both have the same process times. The simulated and experimentally measured results are consistent with those of previous experiments. The processed interstitial iron concentrations measured in this work were 4.5-6$\times 10^{10}$ cm^{-3} for the CZ-Si after processing. Using similar materials and process conditions, Fenning measured approximately 1×10^{11} cm^{-3} processed interstitial iron concentrations [21]. Similarly, both theses found measured final Fe_i for mc-Si of 4-5$\times 10^{10}$ cm^{-3}. The simulated reduction in iron precipitate size after higher temperature processing compared to standard processing is consistent with the synchrotron measurements of Fenning and Zuchlag *et al.* [63], but the particles detected by the synchrotron measurements herein were too small to draw any definitive conclusions about the relative merit of the two processes. Finally, the trends of interstitial iron and minority carrier lifetime described herein are consistent with the simulated and experimental lifetime and iron distribution results of Schön, *et al* [34].

Simulations comparing standard and alternative continuously ramping phosphorus diffusion time-temperature profiles predict that for the same sheet resistance and the same process time, the continuously ramping profile more effectively reduces precipitated and interstitial iron concentrations and increases minority carrier lifetime.

However, μ-XRF measurements of iron precipitate radii do not definitively show that the higher temperature processing of the continuously ramping profile more effectively dissolves iron precipitates than a standard process. Additionally, measurements of the interstitial iron concentration and the minority carrier lifetime did not show a statistically significant difference. For the CZ-Si, simulations of the time temperature profiles predict a difference of 2.3×10^{10} cm^{-3} in final [Fe_i] concentrations, but the standard deviations of the measurements were 3.3 and 4.4×10^{10} cm^{-3}, making the difference not statistically significant with the number of samples and standard deviation of the measurements. Similarly, for the mc-Si, the difference expected by simulation was about 10^9 cm^{-3} while the standard deviation of the measurement is 1.4 and 1.7×10^{10} cm^{-3}. Thus, this constrained comparison of processes with the same sheet resistance and same process time comparison results in a difference that is too small to detect with the number of wafers used in this experiment. Because simulations indicate that the lifetime of the CZ-Si appears to be limited by iron point defects, it is predicted that for the CZ-Si, the addition of extended cool down before unloading the wafers [21] to the continuously ramping profile could result in a detectable reduction in interstitial iron concentration for a similar sheet resistance. For testing the effect on iron precipitates, samples with higher initial precipitated iron concentration may yield more meaningful measurements.

This research focuses on the effect of the phosphorus diffusion time-temperature profile on material quality, but the ability to control process variation is essential for implementation at the industrial scale. The use of one or multiple isothermal steps is ideal for process optimization because the temperature and duration of each step can be adjusted independently of other steps. Continuously ramping profiles have inherently dependent steps. For implementation in industry, the use of several short isothermal steps to approximate a continuously ramping profile may be most effective. Additionally, state of the art diffusion furnaces are designed to accurately control temperature for isothermal steps. The diffusion furnace used in this experiment has a maximum heating rate of 10°C/min and a maximum controlled cooling rate of 3-4°C/min). The temperature gradients in the proposed alternative process here are

harder to control, resulting in varying wafer quality within one run and between runs. This current furnace technology limits solar cell processing to fairly low temperature ramp rates even though simulations indicate that higher temperatures paired with moderately faster ramp rates may produce higher lifetimes in shorter time. This research motivates the development of furnaces that allow for wide temperature ranges, moderate temperature gradients, and high wafer throughput.

Although this novel approach to solar cell processing may be promising at a material level, its effect on solar cell efficiency must be further simulated and experimentally tested. Industrially-relevant higher sheet resistances were measured, but the final solar cell efficiency depends on the actual profiles of phosphorus as a function of depth, which were not measured here. The electrically active phosphorus concentration profile can be measured with electrochemical capacitance voltage measurements, and the total phosphorus concentration profile can be measured with secondary ion mass spectroscopy.

At the simulation development level, the Impurity-to-Efficiency simulator currently makes the simplifying assumption that the concentrations of electrons, electrically active phosphorus, and the sum of electrically active and inactive phosphorus concentrations are equal. According to Bentzen *et al.* [24], at concentrations above 2×10^{19} cm^{-3}, the total phosphorus concentration exceeds the electron and electrically active phosphorus concentration. The current simplification introduces error into the predicted phosphorus profile and may impact the predicted processed iron distribution. Additionally, the expressions for the diffusivity and solubility of iron in p-type silicon are used for the whole thickness of the silicon wafer, including in the heavily phosphorus-doped n-type emitter where the diffusivity is lower and the solubility is higher than in p-type. This pair of simplifications may have a small effect on the average iron distribution and minority carrier lifetime because the emitter is a small fraction of the thickness of the wafer, but it certainly introduces error into the iron precipitation behavior in the emitter [22].

More broadly, further cost modeling is required to quantify the potential for this proposed alternative approach to solar cell processing to reduce the cost/W$_p$ of photo-

voltaic modules. The degree to which this novel processing can reduce costs depends on many factors, including the silicon feedstock characteristics, the baseline solar cell process, the relationship between the marginal improvement in minority carrier lifetime and final solar cell efficiency, and the overall cost structure of the module producer. A back-of-the-envelope calculation indicates that assuming a standard mc-Si scenario at 14.8% module efficiency, a 10% relative increase in efficiency breaks even with a four-fold increase in phosphorus diffusion process time [10]. From this calculation, it is clear that there is room to sacrifice some manufacturing throughput for a gain in solar cell efficiency. This calculation indicates that, if it improves minority carrier lifetime, a slightly extended continuously ramping phosphorus diffusion step may help reduce the cost/W_p of silicon photovoltaics, thereby further enabling the widespread dissemination of the technology.

This research simulated and experimentally tested two different typical crystalline silicon materials for solar cells, and the two materials responded differently to the same processing. Guided by simulation, this research points toward being able to predictively tailor processing to measurable as-grown silicon material characteristics. Tailored processing may enable cost-effective control of the distribution of iron precipitates and point defects and the resulting lifetime and final solar cell efficiency. Finally, the fundamental insights about the coupled kinetics of dopants and impurities during solar cell processing that were also observed in this study can be applied to process development and optimization for novel solar cell materials, including kerfless and n-type silicon.

Chapter 8

Conclusions

With the goal of reducing the cost/W_p of crystalline silicon photovoltaic modules, the effect of two different phosphorus diffusion processes on the distribution of iron impurities was simulated and experimentally tested. Iron in point defect and precipitated form can limit the minority carrier lifetime and ultimately the solar cell efficiency, but the detrimental impact can be mitigated by dissolving precipitated iron and gettering iron point defects to the phosphorus-rich emitter layer or metallic precipitates. A standard and an alternative process with the same process time and similar sheet resistances were designed and tested. The standard process consists of heating from 800°C to 824°C, holding at that temperature while diffusing in phosphorus, then cooling to room temperature. The alternative process consists of heating from 800°C to a higher 882°C, linearly cooling to a moderate temperature of 789°C while diffusing in phosphorus, then cooling to room temperature.

Simulations predict that, compared to the standard process, the alternative process both more effectively dissolves iron precipitates at the higher temperatures and segregates iron point defects to the emitter during the more moderate temperatures, resulting in a higher effective bulk minority carrier lifetime in the same amount of time while achieving a similar sheet resistance. Synchrotron-based μ-XRF measurements of iron precipitates before and after processing were not conclusive due to the small size of the detected iron particles. Additionally, the measured difference in minority carrier lifetime and interstitial iron concentration due to the two processes was not

statistically significant. However, it is expected that the addition of an extended cooling step to the alternative profile to more effectively segregate iron point defects to the emitter could result in a statistically significant reduction in interstitial iron concentration and increase in minority carrier lifetime compared to the standard process while still achieving similar sheet resistances. More heavily iron-contaminated synchrotron samples could clarify the impact of alternative processing on the distribution of iron precipitates.

With current furnace technology, continuously ramping time-temperature profiles that lack any isothermal steps result in more run-to-run process variation because the processing steps are inherently dependent and diffusion furnaces are designed to maintain constant temperatures. Development of diffusion furnaces that can control temperature during faster-ramping heating and cooling steps would enable access to this promising alternative processing parameter space. Additionally, this alternative processing may prove beneficial for processing novel silicon solar cell materials because it is likely that the distribution of metallic impurities still needs to be engineered to enable high-efficiency, cost-effective photovoltaic modules.

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